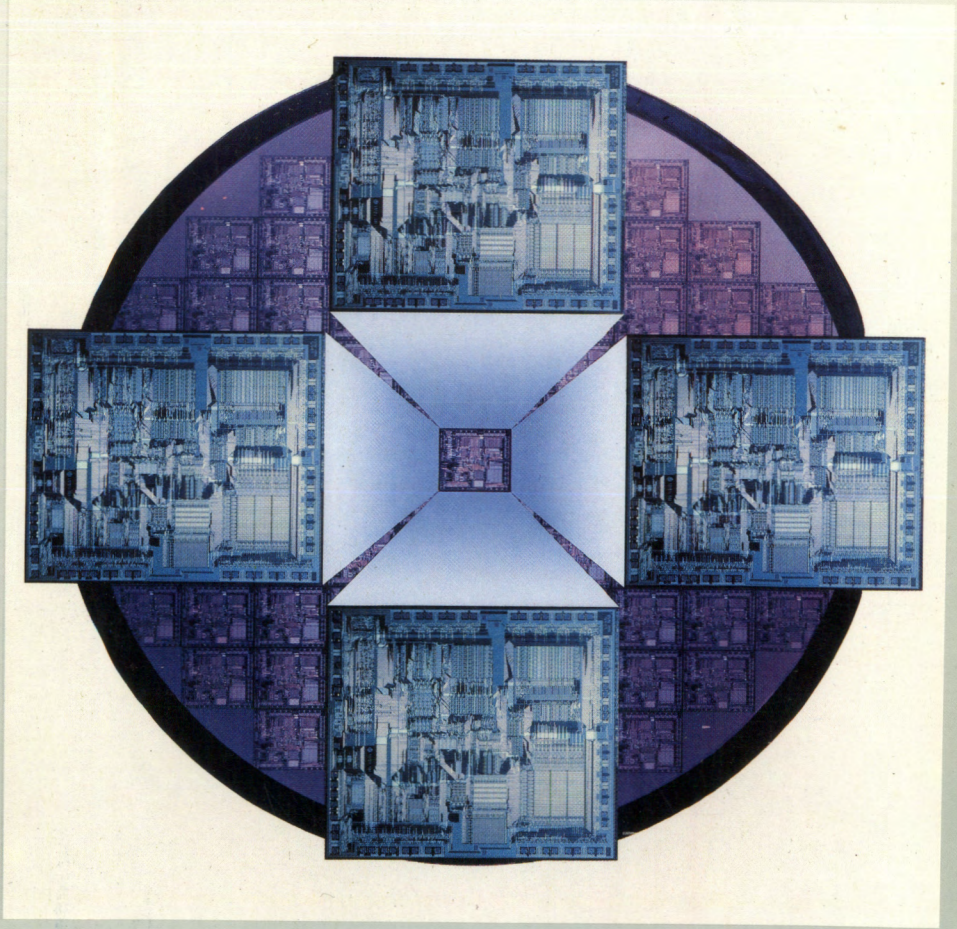
SIEMENS

Microcomputer Components

Peripheral Components and Memories

Data Catalog 1988



Microcomputer Components
Data Catalog 1988

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Siemens Aktiengesellschaft

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Type Survey for Data Catalog
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SAB 82C288	CMOS bus controller for SAB 80286 processor family (16, 20, 25 MHz)
SAB 82289	Bus arbiter for SAB 80286 processor family (12, 16 MHz)

General Information

General Information

Type designation code for ICs

IC type designations are based on the European Pro Electron sytem. The code system is explained in the Pro Electron brochure D 15, edition 1985, available at:

Pro Electron, Avenue Louise, 430 (B. 12)
B-1060 Brussels, Belgium

Mounting instructions

Plastic package

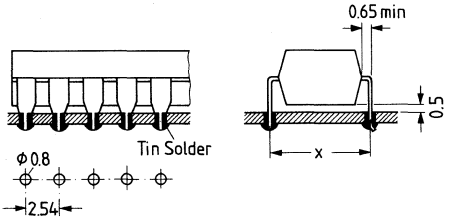
The 90° pins fit into holes with a diameter of 0.7 to 0.9 mm, spaced 2.54 mm apart. See spacing x in figure 1.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1)**.

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for hand soldering and 260°C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

Plastic packages (SO and PLCC) for surface mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s
Wave soldering: (pins and package are dipped into the tin bath)	soldering temperature 260 °C, max. soldering time 8 s

Storage, pretreatment before processing

The components are to be stored in a dry environment. When solder methods causing solder heat shock stresses are used (reflow soldering where the component is dipped into the solder bath, vapor-phase soldering) it is recommendable to subject IC's in plastic packages to a 24-hour drying phase at 125°C.

Other points to note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.
When the pins are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances should the components be removed or inserted while the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

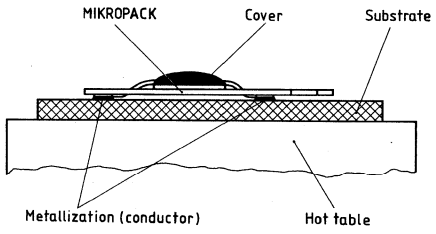
MIKROPACK (SMD)

MIKROPACK components are delivered on film reels.

Mounting suggestions

a) We recommend vapor phase soldering: soldering temperature 215°C, soldering time max. 30 s
b) For prototypes and small quantities (up to approximately 50.0 items/y), the hot table soldering method can also be used (**see figure 2**).

Figure 2



Required equipment and accessories

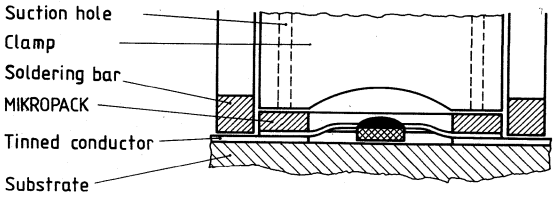
- cutting device
- hot table, temperature regulated (e.g. Weld-Equip, Unitek)
- stereo microscope (e.g. Wild, Zeiss, magnification 6 · · · 40 times)
- substrate material: epoxy resin; hard paper; ceramic (thick thin film)

Soldering data

- soldering temperature: 210 °C max.
- solder coating on substrate: Pb/Sn (e.g. 60/40) wave-tinned or electro-deposited
- soldering time: approx. 10 s
- flux: e.g. colophony, dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

c) For large quantities (e.g. more than 50.0 items/y) bar soldering is also suitable.

Figure 3



Required equipment

- soldering equipment (e.g. Weld-Equip, Farco, Jade)
- substrate material: epoxy resin; hard paper; flexible materials, e.g. polyamide

Soldering data

- soldering temperature: 210 °C max.
- solder coating on the substrate: Pb/Sn (e.g. 60/40), wave-tinned or electro-deposited
- soldering time: approx. 2 s
- flux: e.g. colophony dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

Processing guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (**ESS**) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (**ESD**).

Of the multiple of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
   Means which are effective here are an increase in relative humidity to $\geq$ 60% and the replacement of highly charging plastics by antistatic materials.
b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^8\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer:

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of >50% a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.

4. If conductive floors, $R = 5 \times 10^4$ to $10^7\ \Omega$ are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to $10^7\ \Omega$).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to $10^8\ \Omega$.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) Conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.
   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) Anti-static (transparent) tubes.
   The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to $10^8\ \Omega$/cm) between the tube and the machine.

   The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are likewise unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming inspection

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

Material and mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control cannot be used. Siemens EMI-suppression capacitors of the type B 81711-B31 ...-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. Test sockets must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

Packing of assembled PC boards or flatpack units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/\text{cm} < \rho < 10^{10}\ \Omega/\text{cm}$.

In most cases – especially with humidity of $> 40\%$ – this requirement is fulfilled using simple currugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

It must always be ensured that boards do not touch.

In special cases it may be necessary to provide potection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping of our devices, are available from Laber of Munich.

Ultrasonic cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	$f > 40$ kHz
exposure	$t < 2$ min
alternating sound pressure	$p < 0.29$ bar
sound power	$N < 0.5$ W/cm^2/liter

Data classification

Maximum ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_A = 25$ °C and for the given supply voltage.

Operating range

In the operating range the functions given in the circuit description will be fulfilled.

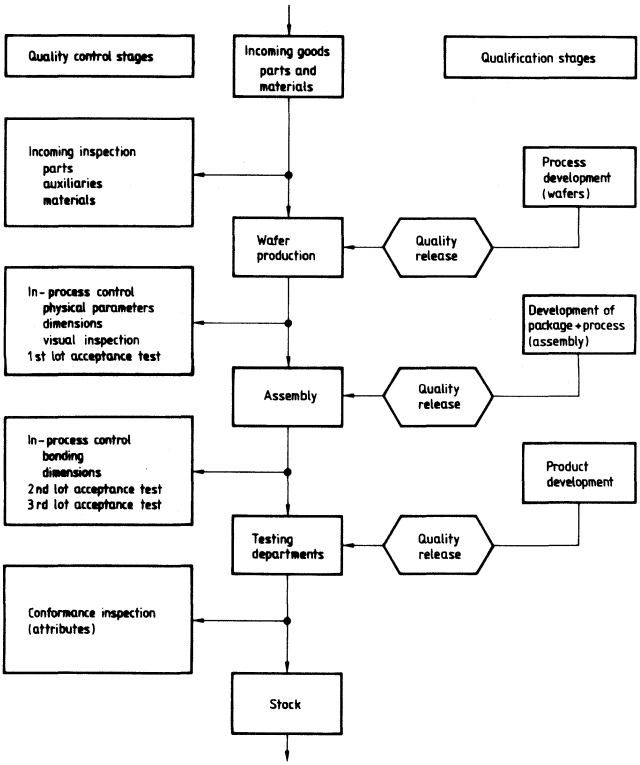
Quality assurance system

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Siemens Quality Assurance System – Integrated Circuits" (SQS-IC).

Figure 4 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

Figure 4



The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs in 1985. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	Sum of electrical defectives AOQ (DPM)	Sum of mechanical defectives AOQ (DPM)
SSI/MSI ≤ 1000 gate functions	40	200	100
LSI/VLSI ≥ 1000 gate functions	120	400	200

Reliability

Measures taken during development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

In-process control during production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

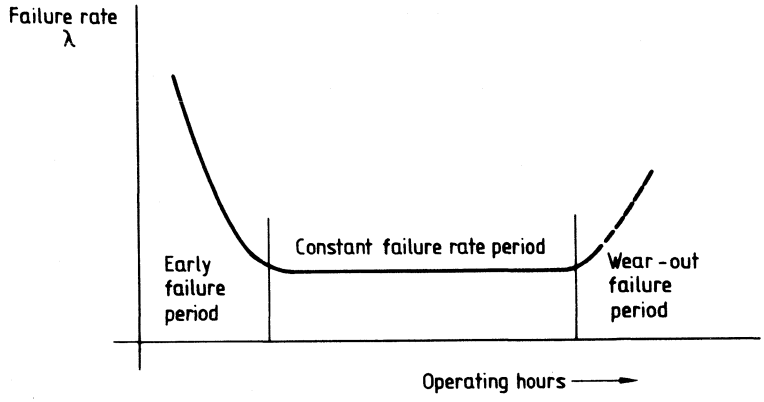
The decreasing failure rates reflect the never ending effort in this direction; they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1985 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

Reliability monitoring

The general course of the IC's failure rate versus time is shown by a so-called "bathtub" curve (**figure 5**). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 5



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp \quad \frac{E_A}{k} \left[\frac{1}{T_1} - \frac{1}{T_2}\right]$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of $T_A = 40\,°C$, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85 °C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

Summary of Types (incl. ordering codes)

Summary of Types (incl. ordering codes)

Type	Ordering code	Package	Function	Page
Peripheral Components				
S SAB 2793B-P	Q67120-Y82	P-DIP-40	Floppy-disk-controller; true data bus, single-sided operation	39
S SAB 2797B-P	Q67120-Y84	P-DIP-40	Floppy-disk-controller; true data bus, double-sided operation	39
S SAB 7201A-P	Q67120-P143	P-DIP-40	Multi-protocol serial communications controller MPSC	69
S SAB 8155-P	Q67120-Q42	P-DIP-40	RAM, stat., with I/O ports and timer, access time 400 ns	105
S SAB 8155-2-P	Q67120-Q86	P-DIP-40	RAM, stat., with I/O ports and timer, access time 300 ns	105
SAB 82C51A-P	Q67120-P216	P-DIP-28	Programmable communications interface	125
S SAB 82C53-P	Q67120-P217	P-DIP-24	Programmable interval timer, command width 400 ns	149
S SAB 82C53-5-P	Q67120-P264	P-DIP-24	Programmable interval timer, command width 300 ns	149
S SAB 82C54-P	Q67120-P212	P-DIP-24	Programmable interval timer, 8 MHz	173
SAB 82C54-1-P	Q67120-P237	P-DIP-24	Programmable interval timer, 10 MHz	173
S SAB 82C55A-2-P	Q67120-P213	P-DIP-40	Programmable peripheral interface	199
S SAB 8256A-P	Q67120-Y43	P-DIP-40	Programmable multifunction controller, MUART, 3 MHz	227
S SAB 8256A-2-P	Q67120-Y59	P-DIP-40	Programmable multifunction controller, MUART, 5 MHz	227
S SAB 8275-P	Q67120-P58	P-DIP-40	Programmable CRT controller, 2 MHz	253
S SAB 8275-2-P	Q67120-P92	P-DIP-40	Programmable CRT controller, 3 MHz	253
S SAB 8276-P	Q67120-P83	P-DIP-40	Small system CRT controller, 2 MHz	281
S SAB 8276-2-P	Q67120-P93	P-DIP-40	Small system CRT controller, 3 MHz	281
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SAB 82520-C	Q67100-H8330	C-DIP-28	High-level serial communications controller, HSCC	323

Type	Ordering code	Package	Function	Page
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SAB 82520-W	Q67100-H8400	PL-CC-28	High-level serial communications controller, HSCC	323
SAF 82520-C	Q67100-H8325	C-DIP-28	High-level serial communications controller, HSCC, −40 to +85°C	323
SAF 82520-P	Q67100-H8512	P-DIP-28	High-level serial communications controller, HSCC, −40 to +85°C	323
SAF 82520-W	Q67100-H8610	PL-CC-28	High-level serial communications controller, HSCC, −40 to +85°C	323
SAB 95C60-12-A	Q67120-P267	C-PGA-145	Quad pixel dataflow manager, 12 MHz	341
SAB 95C60-16-A	Q67120-P268	C-PGA-145	Quad pixel dataflow manager, 16 MHz	341
SAB 95C60-20-A	Q67120-P269	C-PGA-145	Quad pixel dataflow manager, 20 MHz	341

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S HYB 4116-P2	Q67100-Q308	P-DIP-16	RAM, dyn., 16,384 × 1-bit, access time 150 ns	379
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HYB 41256-10	Q67100-Q380	P-DIP-16	RAM, dyn., 262,144 × 1-bit, access time 100 ns	389
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S HYB 511000-10	Q67100-Q362	P-DIP-18	RAM, dyn., CMOS, 1 048,576 × 1-bit, access time 100 ns	405
S HYB 511000-12	Q67100-Q363	P-DIP-18	RAM, dyn., CMOS, 1 048,576 × 1-bit, access time 120 ns	405
S HYB 511000J-85	Q67100-Q375	P-SOJ-26-20	RAM, dyn., CMOS, 1 048,576 × 1-bit, access time 85 ns	405
S HYB 511000J-10	Q67100-Q367	P-SOJ-26-20	RAM, dyn., CMOS, 1 048,576 × 1-bit, access time 100 ns	405
S HYB 511000J-12	Q67100-Q366	P-SOJ-26-20	RAM, dyn., CMOS, 1 048,576 × 1-bit, access time 120 ns	405
HYB 514256-85	Q67100-Q378	P-DIP-18	RAM, dyn., CMOS, 262,144 × 4-bit, access time 85 ns	427
HYB 514256-10	Q67100-Q372	P-DIP-18	RAM, dyn., CMOS, 262,144 × 4-bit, access time 100 ns	427
HYB 514256-12	Q67100-Q373	P-DIP-18	RAM, dyn., CMOS, 262,144 × 4-bit, access time 120 ns	427
HYB 514256J-85	Q67100-Q379	P-SOJ-26-20	RAM, dyn., CMOS, 262,144 × 4-bit, access time 85 ns	427
HYB 514256J-10	Q67100-Q371	P-SOJ-26-20	RAM, dyn., CMOS, 262,144 × 4-bit, access time 100 ns	427
HYB 514256J-12	Q67100-Q370	P-SOJ-26-20	RAM, dyn., CMOS, 262,144 × 4-bit, access time 120 ns	427
SAE 81C80	Q67100-H8390	PL-CC-44	Dual Port RAM, stat., CMOS, 504 byte, −40 to +85°C	447

Peripheral Components

Preliminary

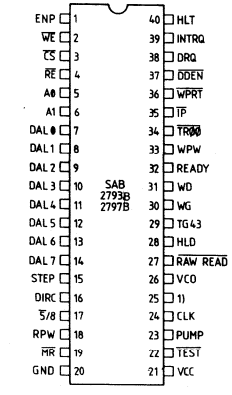
SAB 2793B/2797B Advanced Floppy Disk Formatter/Controller Family

Features	SAB 2793B	SAB 2797B
Single density (FM)	X	X
Double density (MFM)	X	X
True data bus	X	X
Side select output		X
Internal CLK divide	X	

- Improved On-chip PLL data separator
- On-chip write precompensation logic
- Single +5 V supply

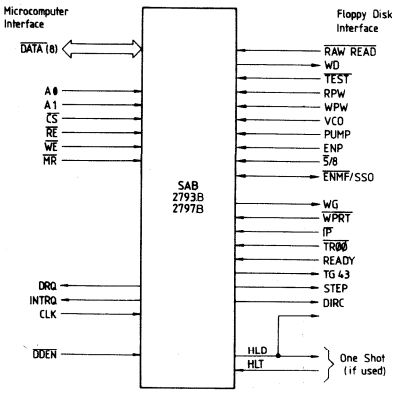
- Accommodates single and double-density formats
  IBM 3740 single density (FM)
  IBM System 34 double density (MFM)
- Automatic seek with verify
- Multiple sector read/write
- TTL-compatible
- Programmable control
  Selectable track-to-track access
  Head load timing
- Software-compatible with the SAB 179X floppy disk formatter/controller family
- Full functional- and pin-compatible to the SAB 2793A/2797A
- Soft sector format compatibility

Pin Configuration



1) SAB 2793B=ENMF
SAB 2797B=SSO

Logic Symbol



The SAB 2793B/2797B are floppy disk controllers in N-channel MOS LSI technology designed to interface with SAB 8080/8085/8051/8086/8088/80186/80188/80286 family processors. Its flexibility and ease of use makes it an ideal floppy disk interface between conventional floppy disks and all computer systems. Software-compatible with its predecessor, the SAB 179X, the device also contains a high-performance phase-lock-loop data separator as well as write precompensation logic.
When operating in double density mode, write precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼ "–8" floppy disk and microfloppy disk interface. 1.87

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
ENP	1	I	ENABLE PRECOMP A logic high on this input enables write precompensation to be performed on the write data output
$\overline{WE}$	2	I	$\overline{WRITE\ ENABLE}$ A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low
$\overline{CS}$	3	I	$\overline{CHIP\ SELECT}$ A logic low on this input selects the chip and enables computer communication with the device
$\overline{RE}$	4	I	$\overline{READ\ ENABLE}$ A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low
AØ, A1	5, 6	I	REGISTER SELECT LINES These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 AØ $\overline{RE}$ $\overline{WE}$ Ø Ø Ø Status register Command register Ø Ø 1 Track register Track register Ø 1 Ø Sector register Sector register Ø 1 1 Data register Data register
DALØ to DAL7	7–14	I/O	DATA ACCESS LINES 8-bit bidirectional bus used for transfer of commands, status and data
STEP	15	O	STEP The step output contains a pulse for each step
DIRC	16	O	DIRECTION Direction output is active high when stepping in, active low when stepping out
$\overline{5/8}$	17	I	5¼", 8" SELECT This input selects the internal VCO frequency for use with 5¼" drives or 8" drives
RPW	18	I	READ PULSE WIDTH An external potentiometer tied to this input controls the phase comparator within the data separator
$\overline{MR}$	19	I	$\overline{MASTER\ RESET}$ A logic low (50 µs min.) on this input resets the device and loads hex 03 into the command register. The "not ready bit" (status bit 7) is reset during $\overline{MR}$ active. When $\overline{MR}$ is brought to a logic high a restore command is executed, regardless of the state of the ready signal from the drive. Also hex 01 is loaded into sector register
$\overline{TEST}$	22	I	$\overline{TEST}$ A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins

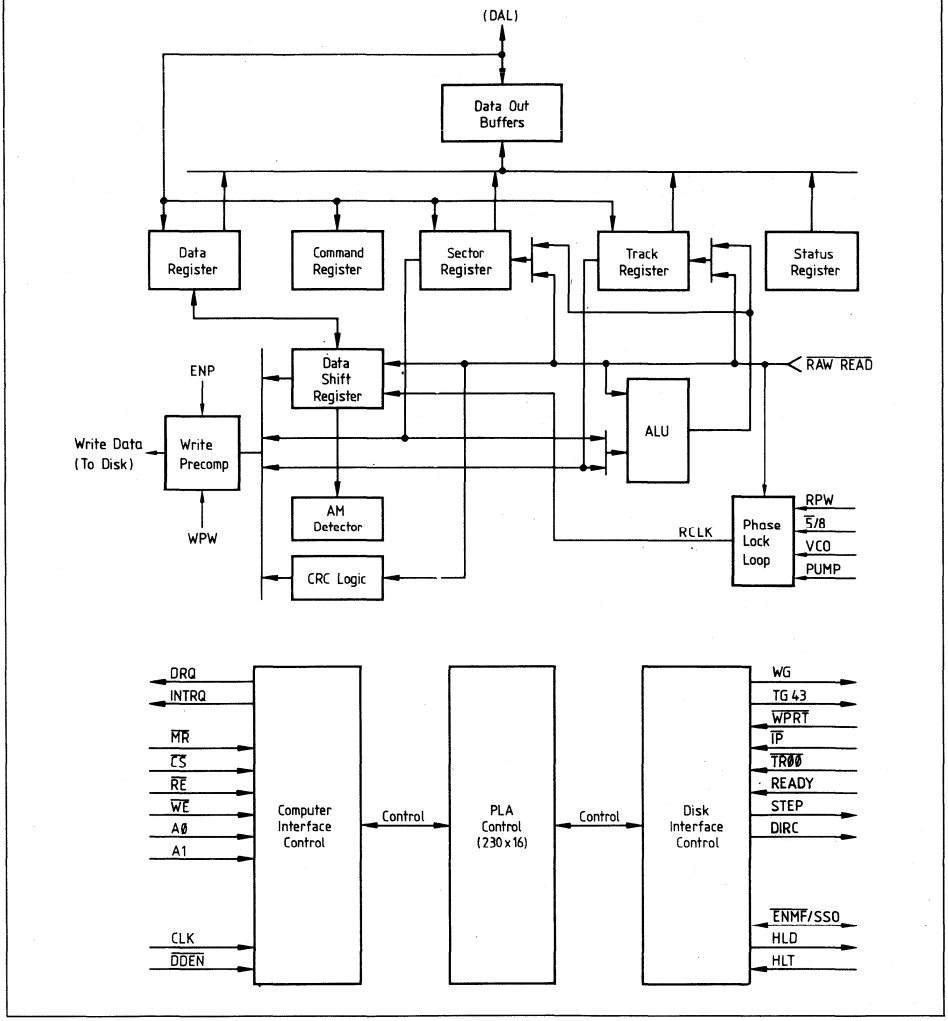
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
PUMP	23	O	PUMP High-impedance output signal which is forced high or low to increase/decrease the VCO frequency
CLK	24	I	CLOCK This input requires a free-running, 50% duty cycle square-wave clock for internal timing reference, 2 MHz ±1% for 8" drives, 1 MHz ±1% for minifloppies
$\overline{\text{ENMF}}$	25	I	$\overline{\text{ENABLE MINIFLOPPY}}$ (SAB 2793B) A logic low on this input enables an internal divide by 2 of the master clock. This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on pin 24, this line must be left open or tied to a logic 1
SSO	25	O	SIDE SELECT OUTPUT (SAB 2797B) The logic level of the side select output is directly controlled by the U flag in type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the sector ID field. If they do not correspond, status bit 4 (RNF) is set. The side select output is only updated at the beginning of a type II or III command. It is forced to a logic 0 upon a master reset condition
VCO	26	–	VOLTAGE CONTROLLED OSCILLATOR An external capacitor tied to this pin adjusts the VCO center frequency
$\overline{\text{RAW READ}}$	27	I	$\overline{\text{RAW READ}}$ The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition
HLD	28	O	HEAD LOAD The HLD output controls the loading of the read/write head against the media
TG43	29	O	TRACK GREATER THAN 43 This output informs the drive that the read/write head is positioned between tracks 44 and 76. This output is valid only during read and write commands
WG	30	O	WRITE GATE This output is made valid before writing is to be performed on the diskette
WD	31	O	WRITE DATA MFM or FM output pulse per flux transition. WD contains the unique address marks as well as data and clock in both FM and MFM formats
READY	32	I	READY This input indicates disk readiness and is sampled for a logic high before read or write commands are performed. If ready is low the read or write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of ready. The ready input appears in inverted format as status register bit 7

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
WPW	33	I	WRITE PRECOMP WIDTH An external potentiometer tied to his input controls the amount of delay in write precompensation mode
$\overline{TR00}$	34	I	$\overline{TRACK\ 00}$ This input informs the SAB 2793B/2797B that the read/write head is positioned over track 00
$\overline{IP}$	35	I	$\overline{INDEX\ PULSE}$ This input informs the SAB 2793B/2797B when the index hole is encountered on the diskette
$\overline{WPRT}$	36	I	$\overline{WRITE\ PROTECT}$ This input is sampled whenever a write command is received. A logic low terminates the command and sets the write protect status bit
$\overline{DDEN}$	37	I	$\overline{DOUBLE\ DENSITY}$ This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected
DRQ	38	O	DATA REQUEST This output indicates that the data register (DR) contains assembled data in read operations, or the DR is empty in write operations. This signal is reset when serviced by the computer through reading or loading the data register
INTRQ	39	O	INTERRUPT REQUEST This output is set at the completion of any command and is reset when the status register is read or the command register is written to
HLT	40	I	HEAD LOAD TIMING When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a single shot triggered by HLD
VCC	21	–	POWER SUPPLY (+5V)
VSS	20	–	GROUND (0V)

Block Diagram



General Description

The SAB 2793B/2797B are N-channel MOS LSI devices performing the functions of a Floppy Disk Formatter/Controller in a single-chip implementation. The SAB 2793B/2797B is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The SAB 2793B/2797B contains all the features of its predecessor, the SAB 179X, plus a high-performance phase-lock-loop data separator as well as write precompensation logic. In double density mode, write precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the SAB 179X and SAB 2793B/2797B designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical in each case, the actual pin assignments vary by only a few pins from any one to another.
The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The SAB 2793B/2797B is set up to operate on a multiplexed bus with other bus-oriented devices. The SAB 2793B/2797B is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads.
The SAB 2797B has a side select output to control double sided drives.

Organization

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register (DSR) – This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during read operations and transfers serial data to the Write Data output during write operations.

Data Register (DR) – This 8-bit register is used as a holding register during disk read and write operations. In disk read operations the assembled data byte is transferred in parallel from the Data Shift Register to the Data Register. In disk write operations information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command the Data Register holds the address of the desired track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register (TR) – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk read, write and verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt command. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device status information. The meaning of the status bits depends on the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cycle Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$
The CRC includes all information starting with the address mark and up to the CRC character. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) – The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control – All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation – Enables write precompensation to be performed on the Write Data output.

Data Separator – A high-performance phase-lock-loop data separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer data, status, and control words out of or into the SAB 2793B/2797B. The DAL are three-state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.
When data transfer with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a read operation or $\overline{WE}$ during a write operation, are interpreted as selector for the following registers:

A1	A0	READ	WRITE
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During direct memory access (DMA) types of data transfers between the Data Register of the SAB 2793B/2797B and the processor, the Data Request (DRQ) output is used for data transfer control. This signal also appears as status bit 1 during read and write operations.
In disk read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters have been lost by having transferred new data into the register prior to processor readout, the Lost Data bit is set in the Status Register. The read operation continues until the end of sector is reached.
In disk write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeros is written on the diskette and the Lost Data bit is set in the Status Register.
Upon completion of every command an INTRQ is generated. INTRQ is reset either by reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.
The SAB 2793B/2797B has two modes of operation depending on the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or at 1 MHz for 5¼" drives.
On the SAB 2793B the $\overline{ENMF}$ input (Pin 25) can be used for controlling both, 5¼" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal divide by 2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both, 5¼" and 8" configurations.
The internal VCO frequency must also be set to the proper value. The $\overline{5}/8$ input (Pin 17) is used to select data separator operation by internally dividing the read clock. When $\overline{5}/8 = 0$, 5¼" drive data separation is selected; when $\overline{5}/8 = 1$, 8" drive data separation is selected.

Clock (24)	$\overline{ENMF}$ (25)	$\overline{5}/8$ (17)	Drive
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

All other conditions are invalid.

Functional Description

The SAB 2793B/2797B is software-compatible with the SAB 179X series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the SAB 179X can be transferred to a SAB 2793B/2797B system without modification.
In addition to the SAB 179X, the SAB 2793B/2797B contains an internal data separator and write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both, data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp single shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second single shot tracks the precomp setting at approximately 3:1 to ensure adequate Write Data pulse widths to meet drive specifications.
Similarly, data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data single shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the read clock output (500 kHz for 8" drives). The VCO trimming capacitor (Pin 26) is adjusted to center frequency.
Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in operation. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the SAB 179X.
Other pins on the device also include pull-up resistors and may be left open to satisfy a logic 1 condition. These are: ENP, 5/8, $\overline{ENMF}$, $\overline{WPRT}$, $\overline{DDEN}$, HLT, $\overline{TEST}$, and $\overline{MR}$.

General Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable either in FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logic 1. For MFM formats, $\overline{DDEN}$ should be placed to a logic 0. Sector lengths are determined at format time by the fourth byte in the ID field.

Sector Length Table*

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

* SAB 2797B may vary – see command summary.

The number of sectors per track as far as the SAB 2793B/2797B is concerned can vary between 1 and 255 sectors. The number of tracks as far as the SAB 2793B/2797B is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 byte with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 byte/sector with 26 sectors/track; or lengths of 1024 byte/sector with 8 sectors/track.

General Disk Write Operation

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the SAB 2793B/2797B before the Write Gate signal can be activated. Writing is inhibited when the Write Protect input is logic low, in which case any write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.
For write operations, the SAB 2793B/2797B provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write Data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

Ready

Whenever a read or write command (Type II or III) is received the SAB 2793B/2797B samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44–76.

Write Precompensation

When operating in double density mode ($\overline{DDEN}$ = 0), the SAB 2793B/2797B has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10k) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.
Setting the write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since the Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

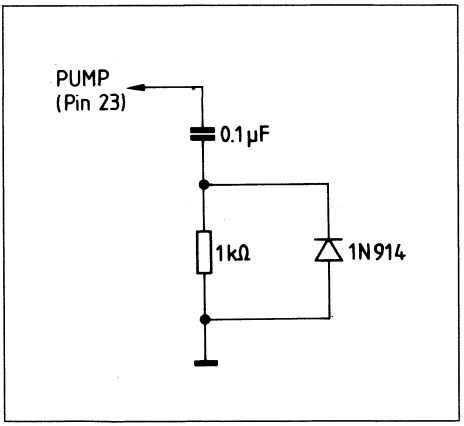
Data Separation

The SAB 2793B/2797B can operate with either an external data separator or its own internal recovery circuit. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.
To program the SAB 2793B/2797B for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e.g. 4.0 MHz for 8" double density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the PUMP output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.
For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a logic 0 for the adjustment procedure.
A 50k Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external, variable capacitor of typically 5 to 60 pF is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate data rate (500 kHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the $\overline{5}/8$ line is held high or the adjustment times above will be doubled.

VCO Operation

After adjustments have been made, the $\overline{TEST}$ pin is returned to a logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.
The PUMP output (Pin 23) consists of positive and negative pulses. Their duration is equivalent to the phase difference of incoming Data versus VCO frequency. This signal is internally connected to the VCO input, but a filter is needed to connect these pulses to a slow moving DC voltage.
The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.
A first-order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as response to normal frequency shift i.e. the lock-up time. A balance must be accomplished between the two conditions to inhibit overresponsiveness to jitter and to prevent an extremely wide lock-up response leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5¼" Drives operate at exactly one-half the data rate (250 Kbyte/s) the above capacitor should be doubled to 0.2 or 0.22 µF.

Command Summary

		Commands for SAB 2793B								Commands for SAB 2797B							
		Bits								Bits							
Type	Command	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0	0	1	1	T	h	V	r_1	r_0
II	Read sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	S	E	C	a_0	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0	1	1	0	1	I_3	I_2	I_1	I_0

Flag Summary

Command Type	Bit	Description
I	r_1, r_0 = Stepping Motor Rate	See page 13 for details
I	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	E = 15 ms Delay	E = 0, No 15 ms delay E = 1, 15 ms delay (30 ms for 1 MHz clock)
II	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	L = Sector Length Flag L = 1 (implicit) for SAB 2793B	
II	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	Ix = Interrupt Conditions Flags I0 = 1: Interrupt on Not Ready to Ready Transition I1 = 1: Interrupt on Ready to Not Ready Transition I2 = 1: Interrupt on Next Index Pulse I3 = 1: Immediate Interrupt Requires a Reset * I3–I0 = 0: Terminate with No interrupt (INTRQ)	

	LSB's Sector Length in ID Field			
	00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

* See Type IV command description for further information.

Status Register Summary

Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 00	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Status for Type I Commands

Bit	Name	Meaning
S7	NOT READY	This bit, when set, indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically ORed with $\overline{MR}$.
S6	WRITE PROTECT	When set, indicates that Write Protect in activated. This bit is an inverted copy of $\overline{WPRT}$ input.
S5	HEAD LOADED	When set, it indicates that the head is loaded and engaged. This bit is a logical AND of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK 00	When set, indicates that Read/Write head is positioned to Track 00. This bit is an inverted copy of the $\overline{TR00}$ input.
S1	INDEX	When set, indicates that index mark is detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0	BUSY	When set, command is in progress. When reset, no command is in progress.

Status for Type II and III Commands

Bit	Name	Meaning
S7	NOT READY	This bit, when set, indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and ORed with $\overline{MR}$. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	For Read Record: not used. For Read Track: not used. On any Write: It indicates a Write Protect. This bit is reset, when updated.
S5	RECORD TYPE	For Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. For any Write: forced to a zero.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates that the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates that the DR is full on a read operation or the DR is empty on a write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

Summary of Adjustment Procedures

Write Precompensation

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19).
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

Data Separator

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19). Ensure that $\overline{5}/8$, and $\overline{\text{DDEN}}$ are set properly.
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for 1/8 of the read clock (250 ns for 8" DD, 500 ns for 5¼" DD, etc.).
6) Observe frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for data rate (500 kHz for 8" DD, 250 kHz for 5¼" DD, etc.).
8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}}$ = 1 whenever a master reset pulse is applied.

Status Register

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits is updated or cleared for the new command. If the Force Interrupt command is received while a current command is under execution, the Busy status bit is reset, and the rest of the status bits is left unchanged. If the Force Interrupt command is received while there is no current command under execution, the Busy Status bit is reset and the rest of the status bits is updated or cleared as after a Type I command.
The user can optionally read the Status Register through program control or by using the DRQ line with DMA or interrupt methods. When the Data Register is read, the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes the reset of both DRQs. The Busy bit in the status may be monitored by a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because reading the Status Register to determine the condition of Busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown on page 11.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 µs	6 µs
Write to Command Reg.	Read Status Bits 1-7	28 µs	14 µs
Write to Any Register	Read from Diff. Register	0	0

Times double when clock = 1 MHz

Command Description

The SAB 2793B/2797B will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The only exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized on page 10.

Type I Commands

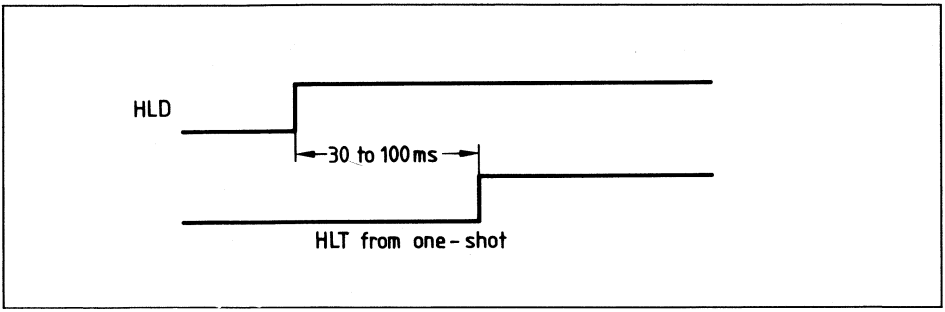
The Type I commands include the Restore, Seek, Step, Step-In and Step-Out commands. Each of the Type I commands contains a rate field (r_0, r_1) which determines the stepping motor rate.
A 2 µs (MFM) or 4 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the Direction output. The chip steps the drive in the same direction it has been stepped previously, unless the command changes direction. The Direction signal is active high when stepping in and low when stepping out. The Direction signal has been valid 12 µs before the first stepping pulse is generated. The rates can be applied to a Step-Direction motor through the device interface.

Stepping Rates

CLK		2 MHz	1 MHz
r1	r0	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step, additional 15 milliseconds of head settling time are generated if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head setting time if the E flag is set in any Type II or III command.
When a Seek, Step or Restore command is executed an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond setting time after the head is loaded against the media. The track number from the first encountered ID field is compared against the contents of the Track Register. If the track numbers correspond and the ID field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC Error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. The SAB 2793B/2797B must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the Seek Error is set and an INTRQ is generated. If V = 0, no verification is performed. The Head Load (HLD) output controls the movement of the Read/Write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the Verify flag is set (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with h = 0 and V = 0, or if the SAB 2793B/2797B is in an idle state (non-busy) and 15 index pulses have occurred.
Head Load timing (HLT) is an input to the SAB 2793B/2797B which is used for the head engage time.
When HLT= 1, the SAB 2793B/2797B assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a single shot. The output of the single shot is then used for HLT and supplied as an input to the SAB 2793B/2797B.

Head Load Timing



When both HLD and HLT are true, the SAB 2793B/2797B will read from or write to the media. The "AND" of HLD and HLT appears as status bit 5 in Type I status.

Summary of the Type I commands:
If h = 0 and V = 0, HLD is reset.
If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay.
If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms delay occurs, and the SAB 2793B/2797B waits for HLT to be true.
If h = 1 and V = 1, HLD is set at the beginning of the command.
Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the SAB 2793B/2797B waits for HLT to occur.
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

Restore (Seek Track 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeros and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r_1 r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeros and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the SAB 2793B/2797B terminates operation, interrupts and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is always executed when $\overline{MR}$ goes from an active to an inactive state.

Seek

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The SAB 2793B/2797B will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command. Note: When using multiple drives, the Track Register must be updated for the drive selected before seek commands are issued.

Step

Upon receipt of this command, the SAB 2793B/2797B issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous Step command. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Step-In

Upon receipt of this command, the SAB 2793B/2797B issues one stepping pulse towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Step-Out

Upon receipt of this command, the SAB 2793B/2797B issues one stepping pulse towards track 0. If the T flag is on, the Track Register is decremented by

one. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading a Type II command into the Command Register the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag is 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 ms delay. If the E flag is 0, the head is loaded and HLT is sampled without a 15 ms delay.
When an ID field is located on the disk, the SAB 2793B/2797B compares the track number on the ID field with the Track Register. If they do not match, the next encountered ID field is read and a comparison is again made. If there has been a match, the Sector Number of the ID field is compared with the Sector Register. If there is no sector match, the next encountered ID field is read off the disk and again compared. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The SAB 2793B/2797B must find an ID field with a track number, sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record-Not-Found status bit is set (Status bit 4) and the command is terminated with an interrupt. Each of the Type II commands contains an m flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the termination of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The SAB 2793B/2797B will continue to read or write multiple records and update the Sector Register in numerical ascending sequence until the Sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.
For example: If the SAB 2793B/2797B is instructed to read sector 27 and there are only 26 sectors on the track, the Sector Register exceeds the number available. The SAB 2793B/2797B will search for 5 disk revolutions, interrupt out, reset Busy, and set the Record-Not-Found status bit.

The Type II commands for the SAB 2793B also contain Side Select Compare flags. When C = 0 (bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the S flag (bit 3). If the S flag corresponds to the side number recorded in the ID field, the SAB 2793B/2797B continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.
The Type II and III commands for the SAB 2797B contains a Side Select flag (bit 1). When U = 0, SSO is updated to 0. Similary, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not correspond within 5 revolutions the interrupt line is made active and the RNF status bit is set.
The SAB 2797B Read Sector and Write Sector commands include an L flag. The L flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the L flag should be set to a one.

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 byte in single density and 43 byte in double density after the last ID field CRC byte; if not, the ID field search is repeated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the read operation, the type of Data Address Mark encountered in the field is recorded in the Status Register (bit 5) as shown:

Status Bit 5	
1	Deleted Data Mark
0	Data Mark

disk. At this time the Data Address Mark is written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The SAB 2793B/2797B counts off 11 bytes in single density and 22 bytes in double density from the CRC field, and the Write Gate (WG) output is made active if the DRQ is serviced (i.e. the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the

The SAB 2793B/2797B then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data status bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of hex FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ is set between 8 and 12 µs after the last CRC byte has been written. For partial sector writing, the proper method is to write the data and fill the balance with zeros. By letting the chip fill the zeros, errors may be masked by the Lost Data status and improper CRC bytes.

Types III Commands

Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read from the disk, and the six data bytes of the ID field are assembled and transferred to the DR. And DRQ is generated for each byte. The six bytes of the ID field are shown below:

Track Address	Side number	Sector address	Sector length	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the SAB 2793B/2797B checks for validity and the CRC Error status bit is set if there is a CRC error. The track address of the ID field is written into the Sector Register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy status bit is reset.

Read Track

Upon receipt of the Read Track command, the head is loaded, and the Busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse.

All gap, header, and data bytes are assembled and transferred to the Data Register. DRQs are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the termination of the command.
This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM. If an address mark does not appear on schedule with the Lost Data status flag being set, the ID AM, ID field, ID CRC bytes, DAM, data and data CRC bytes for each sector will be correct. The gap bytes may be read incorrectly during write splice time because of synchronization.

Write Track Formatting the Disk

Formatting the disk is a comparatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished

by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The data request is activated immediately upon receipt of command, but writing will not start before the first byte is loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated by making the device not busy. The Lost Data status bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted.

This sequence continues from one index mark to the next. Normally, whatever data pattern appears in the Data Register, it is written on the disk with a normal clock pattern. However, if the SAB 2793B/2797B detects a data pattern of F5 thru FE in the Data Register, this is interpreted as Data Address Marks with missing clocks or CRC generation. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern. Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 byte.

Control Bytes for Initialization

Data Pattern in DR (hex)	SAB 2793B/2797B Interpretation in FM ($\overline{DDEN}$ = 1)	SAB 2793B/2797B Interpretation in MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1[1] in MFM, Preset CRC
F6	Not Allowed	Write C2[2] in MFM
F7	Generate 2 CRC Bytes	Generate 2 CRC Bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

[1] Missing clock transition between bits 4 and 5
[2] Missing clock transition between bits 3 and 4

Type IV Commands

The Force Interrupt command is generally used to terminate a multiple sector Read or Write command or to ensure Type I status in the Status Register. This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit set) the command will be terminated and the Busy status bit reset.
The lower four bits of the command determine the conditional interrupt as follows:
I0: Not-Ready to Ready Transition
I1: Ready to Not-Ready Transition
I2: Every Index Pulse
I3: Immediate Interrupt
The conditional interrupt is enabled when the corresponding bit positions of the command (I3–I0) are set to a1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.
If I3–I0 are all set to zero (hex D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status register or writing to the Command Register will not automatically clear the interrupt. The hex D0 is the only command that will enable the immediate interrupt (hex D8) to clear on a subsequent load Command Register or read Status Register operation. Follow a hex D8 with a D0 command. Wait 8 µs (double density) or 16 µs (single density) before issuing a new command after a Force Interrupt command has been issued (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt. Forced interrupt stops any command at the end of an internal microinstruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are completed (CRC calculations, comparisons, etc:). More than one condition may be set at a time. If, for example, the Ready to Not-Ready condition (I1 = 1) and the Every Index Pulse (I2 = 1) are both set, the resultant command will be hex DA. The OR function is performed so that either a Ready to Not-Ready or the next Index Pulse will cause an interrupt condition.

Formats

IBM 3740 Format – 128 Byte/Sector (8")

Shown below is the IBM single-density format with 128 byte/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
26	FF (or 00)
[1] 6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRCs Written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (E5)
1	F7 (2 CRCs Written)
27	FF (or 00)
247[2]	FF (or 00)

IBM System 34 Format – 256 Byte/Sector (8")

Shown in the following table is the IBM double-density format with 256 byte/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
50	4E
[1] 12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 1A)
1	01 (Sector Length)
1	F7 (2 CRCs Written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	Data (E5)
1	F7 (2 CRCs Written)
54	4E
598[2]	4E

[1] Write bracketed field 26 times.
[2] Continue writing until SAB 2793B/2797B interrupts out. Approx. 247 (598) byte.
[3] Optional '00' on SAB 2797B only is allowed.

Recommended – 128 Byte/Sector (Minidiskette)

Shown below is the recommended single-density format with 128 byte/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or 00)
[1] 6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 through 10)
1	00 (Sector Length)
1	F7 (2 CRCs Written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (E5)
1	F7 (2 CRCs Written)
10	FF (or 00)
349[2]	FF (or 00)

Recommended – 256 Byte/Sector (Minidiskette)

Shown below is the recommended double-density format with 256 byte/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
60	4E
[1] 12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 10)
1	01 (Sector Length)
1	F7 (2 CRCs Written)
22	4E
12	00
3	F5 (Write A1)
1	FB (Data Address Mark)
256	Data (E5)
1	F7 (2 CRCs Written)
24	4E
718[2]	4E

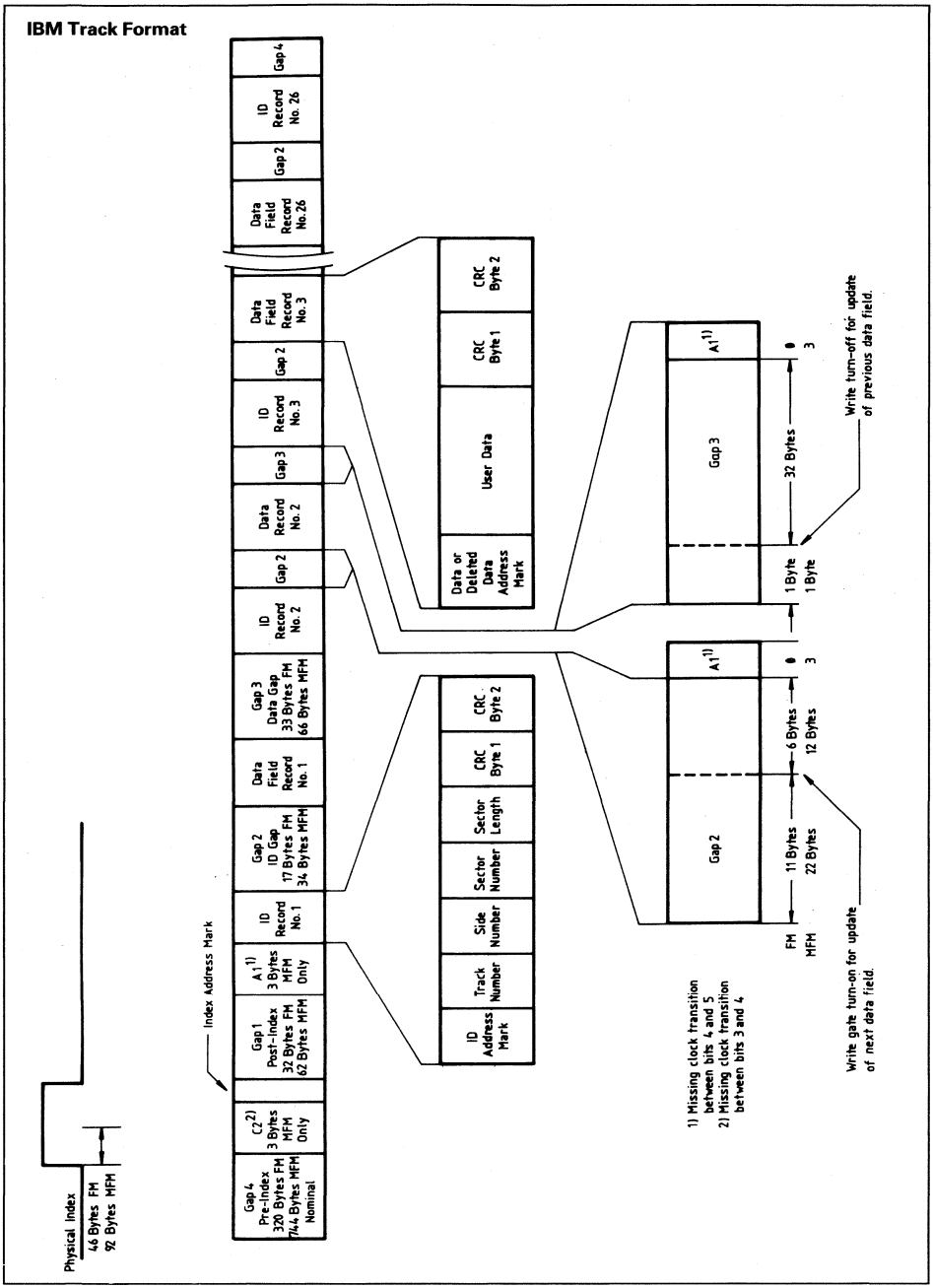
Non-Standard Formats

Variations in the IBM formats are possible to a limited extent if the following requirements are met:
1. Sector size must be 128, 256, 512 or 1024 byte.
2. Gap 2 cannot be varied from the recommended format.
3. 3 bytes of A1 must be used in MFM.

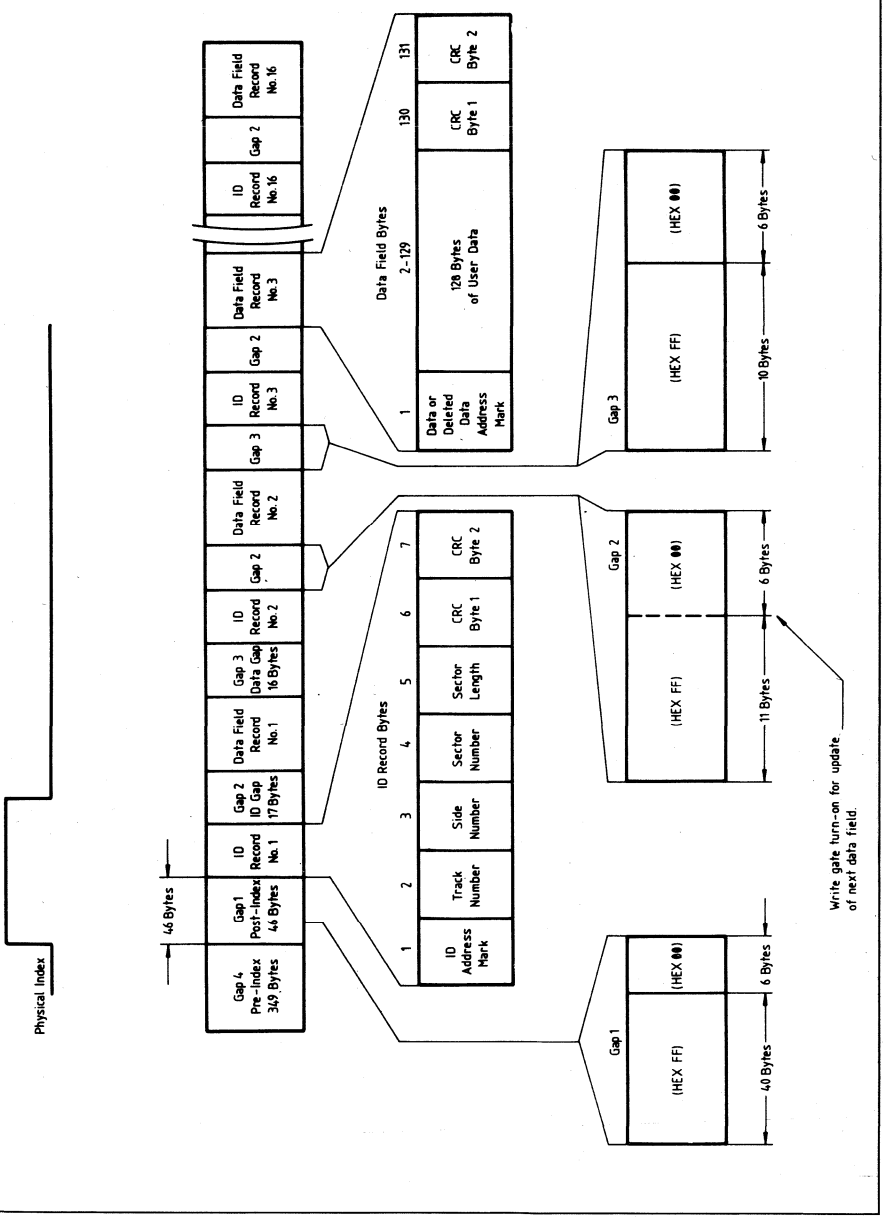
In addition, the Index Address Mark is not required for operation by the SAB 2793B/2797B. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 2793B/2797B operation, however, PLL lock-up time, motor speed variation, write-splice area, etc., will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format should be used for highest system reliability.

	FM	MFM
Gap I	16 Byte FF	32 Byte 4E
Gap II	11 Byte FF	22 Byte 4E
[3]	6 Byte 00	12 Byte 00
		3 Byte A1
Gap III	10 Byte FF	24 Byte 4E
[4]	4 Byte 00	8 Byte 00
		3 Byte A1
Gap IV	16 Byte FF	16 Byte 4E

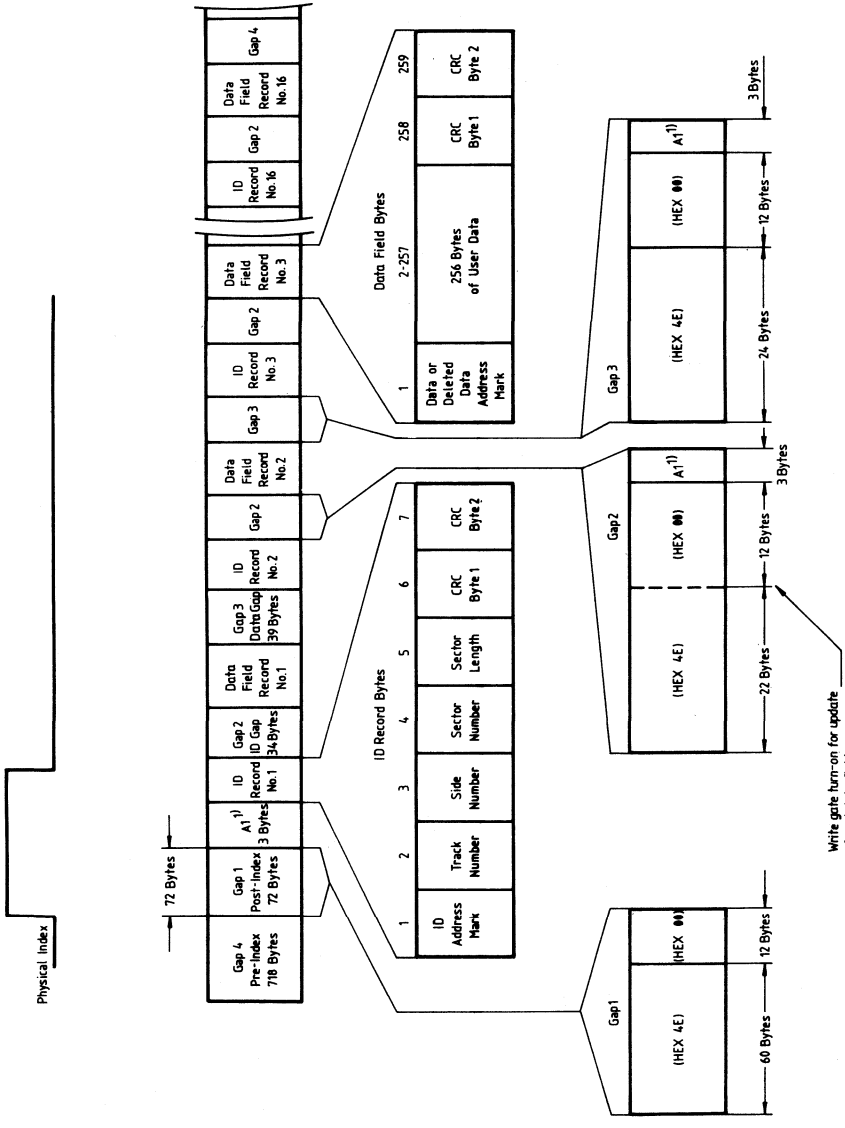
[1] Write bracketed field 16 times.
[2] Continue writing until SAB 2793B/2797B interrupts out. Approx. 349 (718) byte.
[3] Byte counts must be exact.
[4] Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM.


IBM Track Format
Physical Index
46 Bytes FM
92 Bytes MFM
Gap 4 Pre-Index 320 Bytes FM 744 Bytes MFM Nominal
C2) 3 Bytes MFM Only
Gap 1 Post-Index 32 Bytes FM 62 Bytes MFM
A1) 3 Bytes MFM Only
ID Record No. 1
Gap 2 ID Gap 17 Bytes FM 34 Bytes MFM
Data Field Record No. 1
Gap 3 Data Gap 33 Bytes FM 66 Bytes MFM
ID Record No. 2
Gap 2
Data Record No. 2
Gap 3
ID Record No. 3
Gap 2
Data Field Record No. 3
Data Field Record No. 26
Gap 2
ID Record No. 26
Gap 4
Index Address Mark
ID Address Mark
Track Number
Side Number
Sector Number
Sector Length
CRC Byte 1
CRC Byte 2
Data or Deleted Data Address Mark
User Data
CRC Byte 1
CRC Byte 2
A1)
Gap 2
11 Bytes
22 Bytes
A1)
Gap 3
6 Bytes
12 Bytes
3
1 Byte
1 Byte
32 Bytes
3
FM
MFM
1) Missing clock transition between bits 4 and 5
2) Missing clock transition between bits 3 and 4
Write gate turn-on for update of next data field.
Write turn-off for update of previous data field.

Recommended Single-Density Format (Minidiskette)



Recommended Double-Density Format (Minidiskette)



1) F5 writes A1 in MFM with missing clocks between bits 4 and 5.

Absolut Maximum Ratings[1)]

Ambient Temperature Under Bias	0 to + 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to +7V
Power Dissipation	2W

DC Characteristics

TA = 0 to 70°C; VCC = +5%; VSS = 0V

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
IIL 1	Input Leakage Current[2)]	–	–	10	µA	VIN = VCC
IIL 2	Internal Leakage Current[2)]	100	–	1700	µA	VIN = 0V
IOL	Output Leakage Current	–	–	10	µA	VOUT = VCC
VIH	Input High Voltage	2.0	–	–	V	–
VIL	Input Low Voltage	–	–	0.8	V	–
VOH	Output High Voltage	2.4	–	–	V	IOH = −100 µA
VOL	Output Low Voltage	–	–	0.45	V	IOL = 1.6 mA
VOHP	Output High PUMP	2.2	–	–	V	IOHP = −1.0 mA
VOLP	Output Low PUMP	–	–	0.2	V	IOLP = +1.0 mA
ICC	Supply Current	–	70	150	mA	All outputs open

Capacitance[3)]

Symbol	Parameter	Limit Value (max.)	Unit	Test Condition
CIN	Input Capacitance	15	pF	Unmeasured pins returned to GND
COUT	Output Capacitance	15	pF	

[1)] Stresses above those listed under „Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2)] IIL 1 applies to normal inputs, IIL 2 to inputs with internal pull-up resistors on pins 1, 17, 19, 22, 36, 37, and 40. Also pin 25 on SAB 2793B.

[3)] This parameter is periodically sampled and not 100% tested.

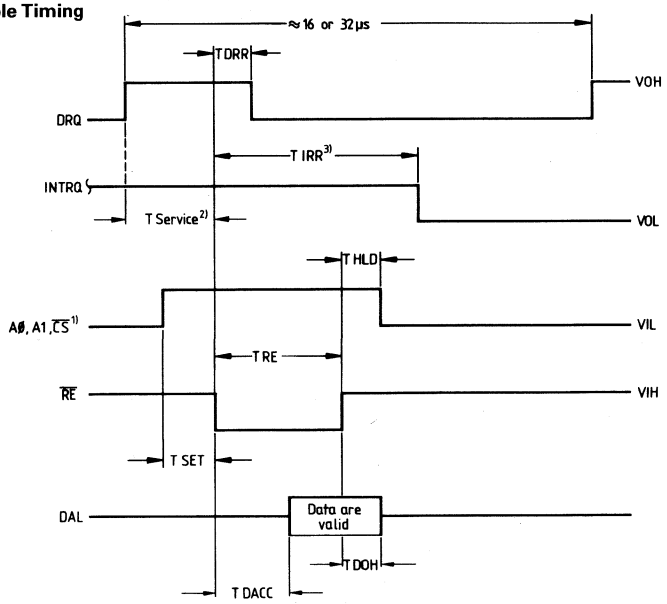
AC Characteristics

TA = 0 to 70°C; VCC = +5V ±5%; VSS = 0V.
All timing readings at VOL = 0.8 V and VOH = 2.0 V.

Read Enable Timing

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
TSET	Setup Addr. and $\overline{CS}$ to $\overline{RE}$	50	–	–	ns	–
THLD	Hold Addr. and $\overline{CS}$ from $\overline{RE}$	10	–	–	ns	–
TRE	$\overline{RE}$ Pulse Width	200	–	–	ns	CL = 50 pF
TDRR	DRQ Reset from $\overline{RE}$	–	100	200	ns	–
TIRR	INTRQ Reset from $\overline{RE}$	–	500	3000	ns	–
TDACC	Data Valid from $\overline{RE}$	–	100	200	ns	CL = 50 pF
TDOH	Data Hold from $\overline{RE}$	20	–	150	ns	CL = 50 pF

Read Enable Timing



DRQ rising edge: Indicates that the data register has assembled data.
DRQ falling edge: Indicates that the data register was read.
INTRQ rising edge: Occurs at end of command.
INTRQ falling edge: Indicates that the status register was read.

1) $\overline{CS}$ may be permanently tied low if desired.

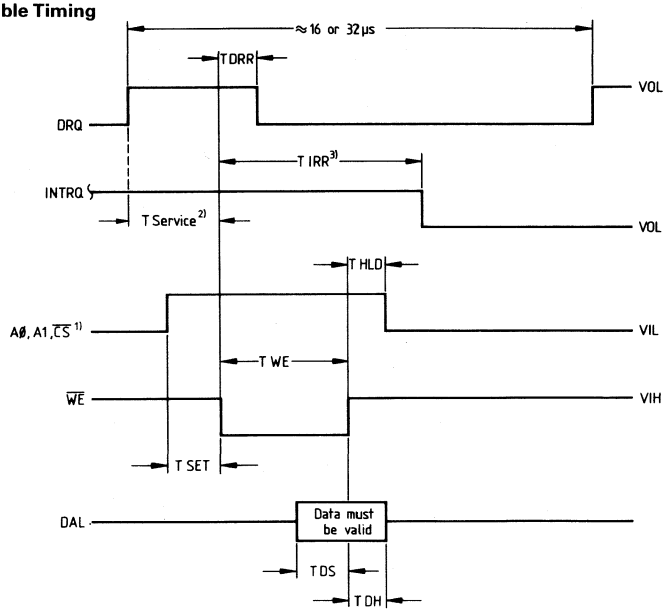
2) T Service (worst case)
– FM = 27.5 µs
– MFM = 13.5 µs

3) Time doubles when CLK = 1 MHz.

Write Enable Timing

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
TSET	Setup Addr. and $\overline{CS}$ to $\overline{WE}$	50	–	–	ns	–
THLD	Hold Addr. and $\overline{CS}$ from $\overline{WE}$	10	–	–	ns	–
TWE	$\overline{WE}$ Pulse Width	200	–	–	ns	–
TDRR	DRQ Reset from $\overline{WE}$	–	100	200	ns	–
TIRR	INTRQ Reset from $\overline{WE}$	–	500	3000	ns	–
TDS	Data Setup to $\overline{WE}$	150	–	–	ns	–
TDH	Data Hold from $\overline{WE}$	50	–	–	ns	–

Write Enable Timing



DRQ rising edge:	Indicates that the data register is empty.
DRQ falling edge:	Indicates that the data register is loaded.
INTRQ rising edge:	Indicates the end of a command.
INTRQ falling edge:	Indicates that the command register is written to.

1) $\overline{CS}$ may be permanently tied low if desired. When writing Data into Sector, Track or Data Register, the User cannot read this register until at least 4 µs in MFM after the rising edge of $\overline{WE}$. When writing into the Command Register status is not valid until some 28 µs in FM/14 µs in MFM later. These times double when CLK = 1 MHz.

2) T Service (worst case); FM = 23.5 µs; MFM = 11.5 µs.

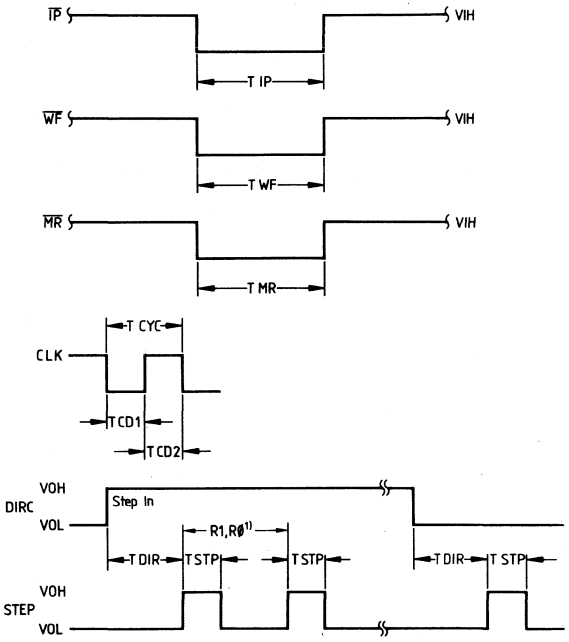
3) Time doubles when CLK = 1 MHz.

Miscellaneous Timings

Symbol	Parameter	Limit Values			Unit	Test Condition	
		Min.	Typ.	Max.			
TCD 1	Clock Duty (low)	230	250	20000	ns	–	
TCD 2	Clock Duty (high)	230	250	20000	ns	–	
TSTP [1]	Step Pulse Output	2 or 4	–	–	µs	–	
TDIR	DIRC Setup to Step	–	12	–	µs	±CLK Error	
TMR	Master Reset Pulse Width	50	–	–	ns	–	
TIP	Index Pulse Width	10	–	–	µs	–	
RPW	Read Window Pulse Width	120 240	– –	700 1400	ns ns	MFM FM ± 15%	Input 0–5V
	Precomp Adjust	100	–	300	ns	MFM	
WPW	Write Data Pulse Width	200	300	400	ns	Precomp = 100 ns MFM	
		600	900	1200	ns	Precomp = 300 ns MFM	
VCO	Free-Running Voltage-Controlled Oscillator	6.0	–	–	MHz	Cext = 0	
	Adjustable by Ext. Capacitor on Pin 26	–	4.0	–	MHz	Cext = 35 pF typ.	
	PUMP Up +25%	5.0	–	–	MHz	PU = 2.4 V, Cext = 35 pF	
	PUMP Down −25%	–	–	3.0	MHz	$\overline{PD}$ = 1.4 V, Cext = 35 pF	
	VCO frequency variation with VCC	–	4.2	–	MHz	VCC=5.25V	VCO=4MHz
		–	3.8	–	MHz	VCC=4.75V	at VCC = 5 V
	VCO frequency variation over temperature	–	4.15	–	MHz	TA = 0°C	TA = 25%
		–	3.75	–	MHz	TA = 70°C	
	Adjustable External Capacitor	15	35	60	pF	VCO = 4.0 MHz rated	
PLL	Lock-up Response	–	–	384	µs	$\overline{5}$/8 = 0	Over specified
		–	–	192	µs	$\overline{5}$/8 = 1	capture range
	Capture Range	0.9	–	1.1	*RCLK	–	
RCLK	Derived Read Clock = VCO: 8, 16, 32	–	500	–	kHz	$\overline{DDEN}$ = 0 $\overline{5}$/8 = 1	VCO = 4.0 MHz
		–	250	–	kHz	$\overline{DDEN}$ = 0 $\overline{5}$/8 = 0	
		–	250	–	kHz	$\overline{DDEN}$ = 1 $\overline{5}$/8 = 1	
		–	125	–	kHz	$\overline{DDEN}$ = 1 $\overline{5}$/8 = 0	
PU/ DON	PU/$\overline{PD}$ Time On (Pulse Width)	–	–	250	ns	MFM	
		–	–	500	ns	FM	

[1] See stepping rates on page 51.

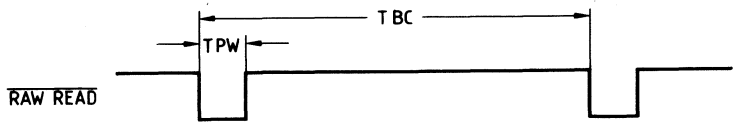
Miscellaneous Timings



Read Data Timing

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
TPW	$\overline{\text{RAW READ}}$ Pulse Width	100	200	–	ns	–
TBC	$\overline{\text{RAW READ}}$ Cycle Time	1500	2000	–	ns	–

Read Data Timing

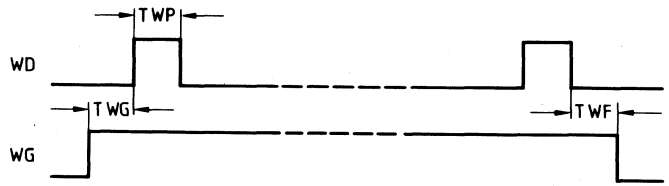


Write Data Timing

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
TWP	Write Data Pulse Width	400	500	600	ns	FM
		200	250	300	ns	MFM
TWG	Write Gate to Write Data	–	2	–	µs	FM
		–	1	–	µs	MFM
TWF	Write Gate from WD	–	2	–	µs	FM
		–	1	–	µs	MFM

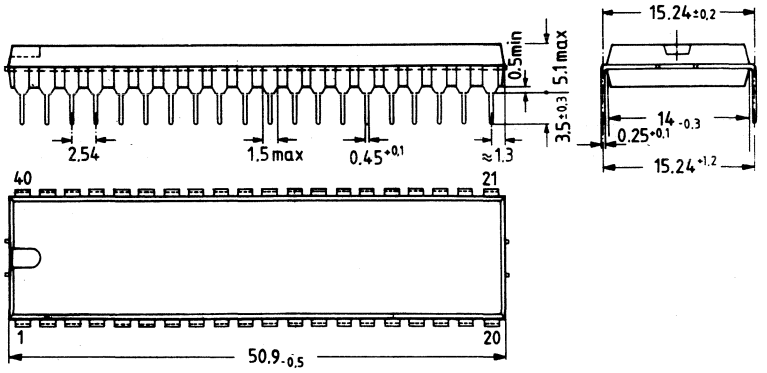
All times double when CLK = 1 MHz; no Write precompensation.

Write Data Timing



Package Outline

Plastic Package, P-DIP, 40 pins



Dimensions in mm

Ordering Information

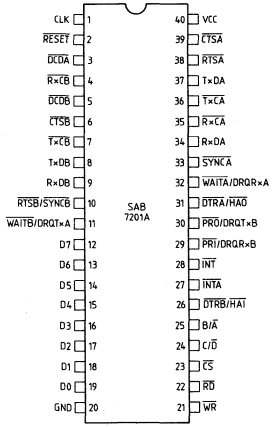
Type	Ordering code	Function
SAB 2793B-P	Q67120-Y82	Floppy disk controller; true data bus, single-sided operation
SAB 2797B-P	Q67120-Y84	Floppy disk controller; true data bus, double-sided operation

Advance Information

SAB 7201A Multi-Protocol Serial Communication Controller

- Two independent full-duplex serial channels
- Four independent DMA channels for transmitted/received data for both serial inputs/outputs
- Modem control signals
- Variable software-programmable data rate, up to 1.25 Mbaud at 5 MHz clock
- Double-buffered transmitter data and quadruple-buffered received data
- Programmable CRC algorithm
- Selection of interrupt, DMA or polling mode
- Asynchronous operation
  - character length: 5, 6, 7, or 8 bits
  - stop bits: 1, 1½, 2
  - clock frequency: x1, x16, x32 or x64 transmission speed
  - parity: odd, even, or disable
  - break generation and detection
  - interrupt on parity, overrun, or framing errors
- Programmable interrupt vectors and interrupt priorities
- Monosync, bisync, and external sync operations
  - software-selectable sync characters
  - automatic sync insertion
  - CRC generation and checking
- HDLC and SDLC operations
  - abort sequence generation and detection
  - automatic zero insertion and detection
  - address field recognition
  - CRC generation and checking
  - I-field residue handling
- High-performance MYMOS technology
- Single +5 V power supply; interfaces most microprocessors including SAB 8080, 8085, 8086, and others
- Single-phase TTL clock
- Available in plastic dual-in line packages

Pin Configuration



Pin Names

CLK	System Clock	DRQTxA DRQTxB DRQRxA DRQRxB	DMA Request, Transmit and Receive, Channel A and B
RESET	Reset		
DCDA DCDB	Data Carrier Detect, Channel A and B		
RxCA RxCB	Receiver Clock, Channel A and B	WAITA WAITB	Wait, Channel A and B
CTSA CTSB	Clear to Send, Channel A and B	D0-D7	Data Bus
		WR	Write
		RD	Read
TxCA TxCB	Transmit Clock, Channel A and B	CS	Chip Select
		C/D	Control/Data Select
		B/A	Channel Select
TxDA TxDB	Transmit Data, Channel A and B	HAI	Hold Acknowledge In
		HAO	Hold Acknowledge Out
RxDA RxDB	Receive Data, Channel A and B	DTRA DTRB	Data Terminal Ready, Channel A and B
SYNCA SYNCB	Synchronization, Channel A and B	INT	Interrupt Request
		INTA	Interrupt Acknowledge
RTSA RTSB	Request to Send, Channel A and B	PRI	Interrupt Priority In
		PRO	Interrupt Priority Out

The Siemens SAB 7201A Multi-Protocol Serial Communication Controller (MPSC) is designed to interface high-speed communications lines using asynchronous, IBM bisync or HDLC/SDLC protocol. It can be interfaced with all Siemens micro-controllers, 8 and 16-bit microprocessors and the SAB 8237 DMA controller in polled, interrupt-driven, or DMA-driven modes of operation. The MPSC is a 40-pin device fabricated using Siemens high-performance MYMOS technology. 5.86

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{TxCA}}$ $\overline{\text{TxCB}}$	7, 36	I	$\overline{\text{TRANSMITTER CLOCK}}$ The transmitter clock controls the rate at which data is shifted out from TxD. The MPSC may be programmed such that the clock rate is 1x, 16x, 32x or 64x the data rate. Data changes on the falling edge of $\overline{\text{TxC}}$. $\overline{\text{TxC}}$ features a Schmitt-trigger input for relaxed rise and fall time requirements (active low).
TxDA TxDB	8, 37	O	TRANSMIT DATA Serial data from the MPSC is output on these pins (marking high).
RxDA RxDB	9, 34	I	RECEIVE DATA Serial data to the MPSC is input on these pins (marking high).
$\overline{\text{SYNCA}}$ $\overline{\text{SYNCB}}$	10, 33	I/O	$\overline{\text{SYNCHRONIZATION}}$ The function of the sync pin depends on the MPSC operating mode. In asynchronous mode, sync is an input that can be read by the processor. Sync can be programmed to generate an interrupt in the same manner as $\overline{\text{DCD}}$ or $\overline{\text{CTS}}$. In external sync mode $\overline{\text{SYNC}}$ is also an input that informs the MPSC when synchronization has been achieved (see the timing waveforms for details). Once synchronization has been achieved, $\overline{\text{SYNC}}$ should be held low until synchronization is lost or a new message is about to start. In internal synchronization modes (monosync, bisync, HDLC/SDLC) $\overline{\text{SYNC}}$ is an output which is active each time a synchronization pattern is recognized. There is no qualifying logic associated with this function. Regardless of character boundaries, $\overline{\text{SYNC}}$ is active on any match (active low).
$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	10, 38	O	$\overline{\text{REQUEST TO SEND}}$ When the MPSC is operated in one of the synchronous modes, $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ are general-purpose outputs that may be set or reset with commands to the MPSC. In asynchronous mode, $\overline{\text{RTS}}$ becomes active as soon as it is programmed on. When programmed off, however, $\overline{\text{RTS}}$ remains active until the transmitter is completely empty. This feature simplifies programming which is required to perform modem control (active low).
DRQTxA DRQTxB DRQRxA DRQRxB	11, 29, 30, 32	O	DMA REQUEST When these lines are active, they indicate to a DMA controller that a transmitter or receiver is requesting DMA data transfer (active high).
$\overline{\text{WAITA}}$ $\overline{\text{WAITB}}$	11, 32	O	$\overline{\text{WAIT}}$ These outputs synchronize the processor with the MPSC when block transfer mode is used. It may be programmed to operate with either the receiver or transmitter, but not with both simultaneously. $\overline{\text{WAIT}}$ is normally inactive. But, for example, if the processor tries to perform an inappropriate data transfer, such as write to the transmitter when the transmitter buffer is full, the $\overline{\text{WAIT}}$ output for the channel is active until the MPSC is ready to accept data. The $\overline{\text{CS}}$, C/$\overline{\text{D}}$, B/$\overline{\text{A}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs must remain stable while $\overline{\text{WAIT}}$ is active (open drain).

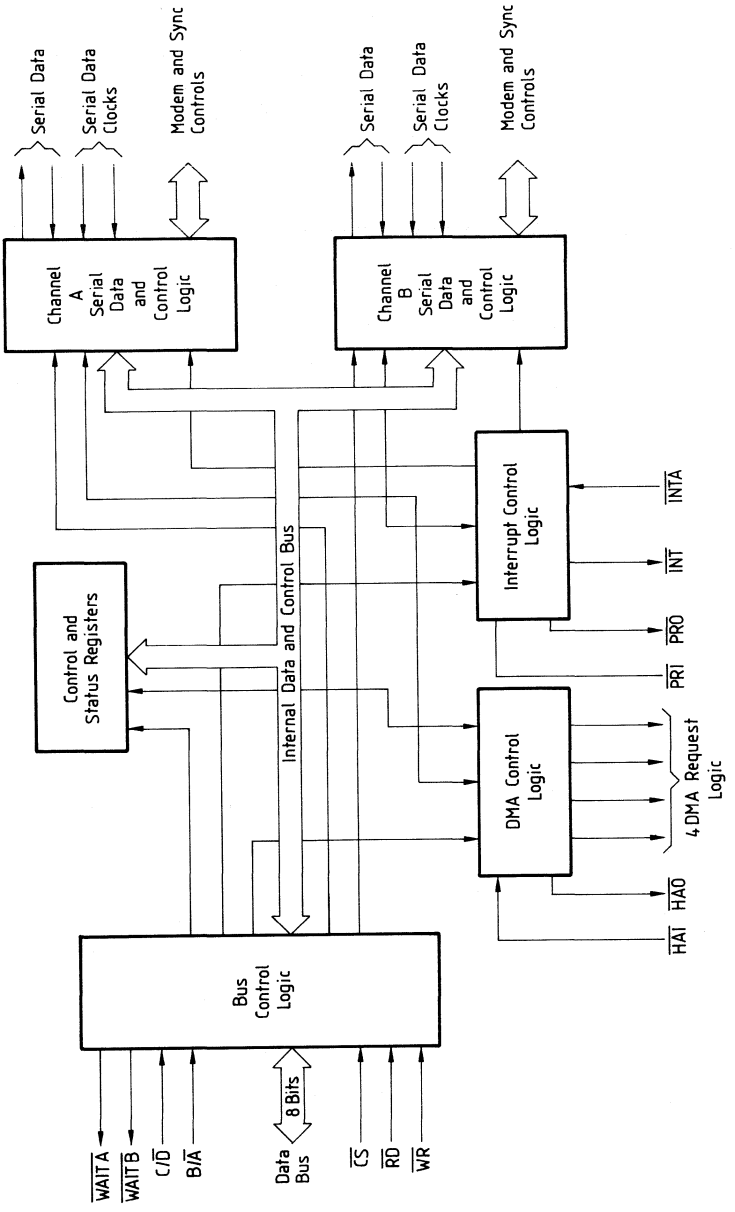
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
D0-D7	12–19	I/O	DATA BUS The data bus lines are connected to the system data bus. Data or status from the MPSC is output on these lines when $\overline{CS}$ and $\overline{RD}$ are active; data or commands are latched into the MPSC with the rising edge of $\overline{WR}$ when $\overline{CS}$ is active (tristate).
$\overline{WR}$	21	I	$\overline{WRITE}$ This input (with either $\overline{CS}$ during read cycle or $\overline{HAI}$ during DMA cycle) activates the MPSC to write data or control information to the device (active low).
$\overline{RD}$	22	I	$\overline{READ}$ This input (with either $\overline{CS}$ during read cycle or $\overline{HAI}$ during DMA cycle) activates the MPSC to read data or status from the device (active low).
$\overline{CS}$	23	I	$\overline{CHIP\ SELECT}$ Chip select allows the MPSC to transfer data or commands during a read or write cycle (active low).
C/$\overline{D}$	24	I	CONTROL/$\overline{DATA\ SELECT}$ This input, together with $\overline{RD}$, $\overline{WR}$ and B/$\overline{A}$, selects the data register (C/$\overline{D}$ = 0) or the control and status registers (C/$\overline{D}$ = 1) for access over the data bus.
B/$\overline{A}$	25	I	CHANNEL SELECT A low signal selects channel A and a high selects channel B for access during a read or write cycle.
$\overline{HAI}$	26	I	$\overline{HOLD\ ACKNOWLEDGE\ IN}$ This input informs the MPSC that the host processor has acknowledged the DMA request and has placed itself in the hold state. The MPSC then performs a DMA cycle for the highest-priorty outstanding DMA request, if there is any (active low).
$\overline{DTRA}$ $\overline{DTRB}$	26, 31	O	$\overline{DATA\ TERMINAL\ READY}$ The $\overline{DTR}$ pins are general-purpose outputs which may be set or reset with commands to the MPSC (active low).
$\overline{INTA}$	27	I	$\overline{INTERRUPT\ ACKNOWLEDGE}$ The processor generates two or three $\overline{INTA}$ pulses (depending on the processor type) to signal all peripheral devices that an interrupt acknowledge sequence takes place. During the interrupt acknowledge sequence, the MPSC, if programmed so, puts information on the data bus to vector the processor to the appropriate interrupt service location (active low).
$\overline{INT}$	28	O	$\overline{INTERRUPT\ REQUEST}$ $\overline{INT}$ is pulled low when an internal interrupt request is accepted (active low, open drain).

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{PRI}$	29	I	$\overline{INTERRUPT\ PRIORITY\ IN}$ This input informs the MPSC that the highest priority device is requesting interrupt. It is used with $\overline{PRO}$ to form a priority-resolution daisy chain when there is more than one interrupting device. The state of $\overline{PRI}$ and the programmed interrupt mode determine the MPSC's response to an interrupt acknowledge sequence (active low).
$\overline{PRO}$	30	O	$\overline{INTERRUPT\ PRIORITY\ OUT}$ This output is active when $\overline{HAI}$ is active and the MPSC is not requesting interrupt ($\overline{INT}$ is inactive). The active state informs the next lower priority device that there are no higher priority interrupt requests pending during an interrupt acknowledge sequence (active low).
$\overline{HAO}$	31	O	$\overline{HOLD\ ACKNOWLEDGE\ OUT}$ This output with $\overline{HAI}$ implements a priority daisy chain for multiple DMA devices. $\overline{HAO}$ is active when $\overline{HAI}$ is active and there are no DMA requests pending in the MPSC (active low).
VCC	40	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Functional Description

The SAB 7201A is a dual-channel multi-protocol serial communication controller designed to satisfy a wide variety of serial data communications applications in computer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller and within that range it can be configured by system software so its features can be optimized for the individual application.

The SAB 7201A is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for other applications than data communications.

The SAB 7201A can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls on both channels. In applications where these controls are not needed the modem controls can be used for general-purpose I/O.

Programming the MPSC

Software operation of the MPSC is very straightforward. Its consistent register organization and high-level command structure help minimize the number of operations required to implement complex protocol designs. Programming is further simplified by the MPSC's extensive interrupt and status reporting capabilities. This section is divided into two parts.

Reset

When the SAB 7201A RESET line is activated, both MPSC channels enter the idle state. The serial output lines are forced to the marking state (high) and the modem interface signals ($\overline{RTS}$, $\overline{DTR}$) are forced high. In addition, the pointer registers are set to zero.

The MPSC Registers

The MPSC interfaces to the system software with a number of write and read registers associated with each channel. Commonly used commands and status bits are accessed directly through write and read register 0. Other functions are accessed indirectly with a register pointer to minimize the address space that must be dedicated to the MPSC.

Write Registers

Write Register	Function
0	Frequently used commands and register pointer control
1	Interrupt control
2	Processor/bus interface control
3	Receiver control
4	Mode control
5	Transmitter control
6	Sync/address character
7	Sync character

Read Registers

Read Register	Function
0	Buffer and "external/status" status
1	Received character error and special condition status
2	Interrupt vector (channel B only)
3	Tx length register, low byte
4	Tx length register, high byte

All write and read registers except RR2 are maintained separately for each channel. Write and read registers 2 are linked with the overall operation of the MPSC and have different meaning when addressed through different channels.

When initializing the MPSC, write register 2A (and 2B if desired) should be programmed first to establish the MPSC processor/bus interface mode. Each channel may then be programmed to being used separately, beginning with write register 4 to set the protocol mode for that channel. The remaining registers may then be programmed in any order.

Command/Status Description

The following command and status bytes are used during initialization and execution phases of operation. All command/status operations on the two channels are identical and independent, unless otherwise noted.

Detailed Register Description

Write Register 0 (WR0)

D7	D6	D5	D4	D3	D2	D1	D0
CRC Control Command		Command			Register Pointer		

D2,D1,D0 Register pointer

The register pointer determines which write register the next byte is to be written into, or which read register the next byte is to be read from. After a hardware or software reset the register pointer is set to zero. Therefore, the first control byte goes to write register 0. When the register pointer is set to a value other than zero the next control or status ($C/\overline{D} = 1$) access is to the specified register, afterwards the pointer is reset to zero. Other commands can freely be combined in write register 0 by setting the register pointer.

D5, D4, D3 Commands

Commands commonly used during the operation of the MPSC are grouped in write register 0. They include the following:

000 **Null:** This command has no effect and is used only to set the register pointer or issue a CRC command.

001 **Send abort:** When operating in the HDLC/SDLC mode this command causes the MPSC to transmit the HDLC/SDLC abort code, issuing 8 to 13 consecutive ones. Any data currently in the transmitter or transmitter buffer is destroyed. After sending the abort the transmitter reverts to the idle phase (flags). When using the Tx byte count-mode enable (D6 of WR1) and an underrun condition occurs, the SAB 7201A will automatically issue the 'send abort' command.

010 **Reset external/status interrupts:** When the external/status change flag is set, the conditions of bits D7 to D3 of read register 0 are latched to allow the capture of the short pulses that may occur. The "reset external/status interrupts" command reenables the latches so that new interrupts may be sensed.

011 **Channel reset:** This command has the same effect on a single channel as an external reset at pin 2. A 'channel reset' command to channel A resets the internal interrupt prioritization logic. This does not occur when a channel reset command is issued to channel B. All control registers associated with the channel to be reset must be reinitialized. After a channel reset, wait at least four system clock cycles before writing new commands or controls to that channel.

100 **Enable interrupt on next character:** When operating the MPSC in an interrupt-on-first-received-character mode this command may be issued at any time. It must be issued at the end of a message to reenable the interrupt logic for the next character received (the first character of the next message).

101 **Reset pending transmitter interrupt/DMA request:** A pending transmitter-buffer-becoming-empty interrupt or DMA request can be reset without sending another character by issuing this command (typically at the end of a message). A new transmitter-buffer-becoming-empty interrupt or DMA request is not performed until another character has been loaded and transferred to the transmitter shift register or when, if operating in the synchronous or HDLC/SDLC modes, the first CRC character has been sent.

110 **Error reset:** This command resets a special receive condition interrupt. It also reenables the parity and overrun error latches that allow errors at the end of a message to be checked.

111 **End of interrupt (channel A only):** Once an interrupt request has been issued by the MPSC all lower priority internal and external interrupts in the daisy chain are held back to permit the current interrupt to be serviced while allowing higher priority interrupts to occur. At some point in the interrupt service routine (generally at the end), the 'end of interrupt' command must be issued to channel A to reenable the daisy chain and allow occurring of any pending lower priority internal interrupt requests. The EOI command must be sent to channel A for interrupts that occurred on either channel.

D7, D6 **CRC control commands:** The following commands control the operation of the CRC generator/checker logic.

00 **Null:** This command has no effect and is used when issuing other commands or setting the register pointer.

01 **Reset receiver CRC checker:** This command resets the CRC checker to zero when the channel is in a synchronous mode, and resets to all ones when in an HDLC/SDLC mode.

10 **Reset transmitter CRC generator:** This command resets the CRC generator to zero when the channel is in synchronous mode, and resets to all ones when in an HDLC/SDLC mode.

11 **Reset Tx underrun/EOM latch:** This command resets the Tx underrun/EOM latch, so when a transmitter underrun condition occurs (that means the transmitter has no more characters to send) the transmitter enters the CRC phase of operation and begins to send the 16-bit CRC character calculated up to that point. The latch is then set, so if the underrun condition persists, idle characters are sent following the CRC. After a hardware or software reset the latch is in the set state. This latch is automatically reset after the first character has been loaded into the Tx buffer in the HDLC/SDLC mode.

Write Register 1 (WR1)

D7	D6	D5	D4	D3	D2	D1	D0
Wait Function Enable	Tx Byte Count Mode Enable	Wait on Receiver/ Transmitter	Receiver Interrupt Mode		Condition Affects Vector	Transmitter Interrupt Enable	Ext./Status INT Enable

Tx Length Register (high and low)

D7	D6	D5	D4	D3	D2	D1	D0
Tx Length Register (low byte)							

D7	D6	D5	D4	D3	D2	D1	D0
Tx Length Register (high byte)							

D0 **External/status interrupt enable:** When this bit is set to one the MPSC issues an interrupt whenever any of the following conditions occurs:
- transition on the $\overline{DCD}$ input pin
- transition on the $\overline{CTS}$ input pin
- transition on the $\overline{SYNC}$ input pin
- entering or leaving synchronous hunt phase, break detection or termination
- HDLC/SDLC abort detection or termination
- idle/CRC latch becoming set (CRC being sent)
- after ending flag is sent in the HDLC/SDLC mode

D1 **Transmitter interrupt/DMA enable:** When this bit is set to one the MPSC issues an interrupt when:
1) The character currently in the transmitter buffer is transferred to the shift register (transmitter buffer becoming empty) or,
2) the transmitter enters the idle phase and begins transmitting sync or flag characters, or
3) the Tx byte count mode enable bit is set (WR1–D6=1). The SAB 7201A will automatically issue a Tx interrupt or DMA request when the transmitter becomes enabled (WR5–D3=1).

D2 **Status affects vector (programmed in channel B for both channels):** When this bit is set to zero the fixed vector programmed in WR2B during MPSC initialization is returned in an interrupt acknowledge sequence. When this bit is set to one the vector is modified to reflect the condition that caused the interrupt.

D4, D3 **Receiver interrupt mode:** This field controls how the MPSC's interrupt/DMA logic handles the "character received" condition.

00 **Receiver interrupts/DMA request disabled:** The MPSC does not issue an interrupt or a DMA request when a character has been received.

01 **Interrupt on first received character only:** In this mode the MPSC issues an interrupt only for the first character received after an "enable interrupt on next character" command (WR0) has been given. If the channel is in a DMA mode, a DMA request is issued for each character received including the first one. This mode generally is used whenever the MPSC is in a DMA or block transfer mode. This will signal the processor that the beginning of an incoming message has been received.

10 **Interrupt (and issue a DMA request) on all received characters:** In this mode an interrupt (and DMA request if the DMA mode is selected) is issued whenever there is a character present in the receiver buffer. A parity error is considered a special receive condition.

11 **Interrupt (and issue a DMA request) on all received characters:** This mode is the same as the one above except that a parity error is not considered a special receive condition. The following are considered special receive conditions:
- receiver overrun factor
- asynchronous framing error
- parity error (if specified)
- HDLC/SDLC end of message (final flag received)

D5 **Wait on receiver/transmitter:** If the wait function is enabled for block transfers, setting this bit to zero causes the MPSC to issue a wait ($\overline{\text{WAIT}}$ output goes low) when the processor attempts to write a character to the transmitter while the transmitter buffer is full. Setting this bit to one causes the MPSC to issue a wait when the processor attempts to read a character from the receiver while the receiver buffer is empty.

D6 **Tx byte count mode enable:** Each channel has a 16-bit Tx length register used for automatic transmit termination. When this bit is set to one the next two consecutive command cycle writes will be to the Tx length register. The first byte is loaded into the lower 8 bits and the second to the upper 8 bits of the Tx length register. The Tx length register holds the number of transfers to be performed by the transmitter. The Tx byte counter (RR3, RR4) is incremented each time a transfer is performed until the value of the Tx byte counter is equal to the value in the Tx length register. When equal, interrupts or DMA requests will be stopped until the Tx byte count enable bit is issued and a new byte count is loaded into the Tx length register. If a transmit underrun occurs in the HDLC/SDLC mode and the Tx byte counter is not equal to the Tx length register contents, the abort sequence will be sent automatically. Also, when using the Tx byte count mode, a transmit interrupt or DMA request will automatically become active after issuing the "Tx enable" command to WR5.
The Tx byte count mode can be cleared by either a channel reset command or a hardware reset.

D7 **Wait function enable:** Setting this bit to one enables the wait function which is described in WR1.

Write Register 2, Channel A (WR2A)

D7	D6	D5	D4	D3	D2	D1	D0
Pin 10 $\overline{\text{SYNCB}}$/ RTSB	RxINT Mask	Interrupt Vector Mode			Priority	DMA Mode Select	

D1, D0 **DMA mode select:** Setting this field determines whether channel A or B is used in a DMA mode (i.e. data transfers are performed by a DMA controller) or in a non-DMA mode where transfers are performed by the processor in either a polled, interrupt, or block transfer mode. The functions of some MPSC pins are also controlled by this field.

D2 **Priority:** This bit selects the relative priorities of the various interrupt and DMA conditions according to the application requirements.

	INT/DMA Mode		Pin Function						Priority
D2 D1 D0	Channel A	Channel B	$\overline{\text{WAITA}}$/DRQRxA $\overline{\text{WAITB}}$/DRQTxA		$\overline{\text{PRI}}$/DRQRxB $\overline{\text{PRO}}$/DRQTxB		$\overline{\text{DTRB}}$/$\overline{\text{HAI}}$ $\overline{\text{DTRA}}$/$\overline{\text{HAO}}$		High Low
0 0 0	INT	INT	$\overline{\text{WAITA}}$	$\overline{\text{WAITB}}$	$\overline{\text{PRI}}$	$\overline{\text{PRO}}$	$\overline{\text{DTRB}}$	$\overline{\text{DTRA}}$	RxA TxA RxB TxB E/SA E/SB
1 0 0	INT	INT							RxA RxB TxA TxB E/SA E/SB
X 0 1	DMA		DRQRxA	DRQTxA	$\overline{\text{PRI}}$	$\overline{\text{PRO}}$	$\overline{\text{HAI}}$	$\overline{\text{HAO}}$	RxA TxA
		INT							RxA* RxB TxB E/SA* E/SB
0 1 0	DMA	DMA	DRQRxA	DRQTxA	DRQRxB	DRQTxB	$\overline{\text{HAI}}$	$\overline{\text{HAO}}$	RxA TxA RxB TxB
									RxA* RxB* E/SA* E/SB*
1 1 0	DMA	DMA							RxA RxB TxA TxB
									RxA* RxB* E/SA* E/SB*
X 1 1	DMA	DMA					$\overline{\text{DTRB}}$	$\overline{\text{DTRA}}$	No Priority
									RxA* RxB* E/SA* E/SB*

*) The E/S interrupt and Rx interrupt may occur in DMA.

D5 to D3 **Interrupt vector mode:** This field determines how the MPSC responds to an interrupt acknowledge sequence from the processor.

Interrupt Acknowledge Sequence Response

	Mode	Read Register 2B and Interrupt Vector Bits Affected when Condition-Affects-Vector Is Enabled
000	Nonvectored	D4 D3 D2
001	Nonvectored	D4 D3 D2
010	Nonvectored	D2 D1 D0
011	Illegal	–
100	8085 Master	D4 D3 D2
101	8085 Slave	D4 D3 D2
110	8086	D2 D1 D0
111	8085/8259A Slave	D4 D3 D2

D6 **RxINT mask:** This option is generally used in the DMA modes. Enabling this bit inhibits the interrupt from occurring when mode "interrupt/DMA request on first received character" is selected. In other words, only a DMA request will be generated when the first character is received.

D7 **Pin 10 $\overline{\text{SYNCB}}$/$\overline{\text{RTSB}}$ select:** Programming a zero into this bit selects $\overline{\text{RTSB}}$ as the function of pin 10. A one selects $\overline{\text{SYNCB}}$.

Write Register 2, Channel B (WR2B)

D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Vector							

D7 to D0 **Interrupt vector:** When the MPSC is used in the vectored interrupt mode the contents of this register is put on the bus during the appropriate portion of the interrupt acknowledge sequence. Its value is modified if status-affects-vector is enabled. The value of RR2B can be read at any time. This feature is particularly useful for determining the cause of an interrupt when the MPSC is used in a nonvectored interrupt mode.

Write Register 3 (WR3)

D7	D6	D5	D4	D3	D2	D1	D0
Number of Received Bits per Character		Auto-Enable	Enter Hunt Phase	Receiver CRC Enable	Address Search Mode	Sync Character Load Inhibit	Receiver Enable

D0 **Receiver enable:** After the channel has been completely initialized, setting this bit to one allows the receiver to begin operation. This bit may be set to zero at any time to disable the receiver.

D1 **Sync character load inhibit:** In the character synchronous modes, this bit inhibits the transfer of sync characters to the receiver buffer thus performing a "sync-stripping" operation. When using the MPSC's CRC checking ability this feature should be used only to strip leading sync characters preceding a message, since the load inhibit does not exclude sync characters embedded in the message from the CRC calculation. Synchronous protocols using other types of block checking such as checksum or LRC are free to strip embedded sync characters with this bit.

D2 **Address search mode:** In the HDLC/SDLC mode, setting this bit places the MPSC in an address search mode. Character assembly does not begin until the 8-bit character (secondary address field) following the starting flag of a message matches either the address programmed into WR6 or the global adress 1111 1111.

D3 **Receiver CRC enable:** This bit enables (=1) and disables (=0) the CRC checker in the COP mode, allowing characters from the CRC calculation to be selectively included or excluded. The MPSC features a one-character delay between the receiver shift register and the CRC checker so that the enabling or disabling takes place at the same time the last character is transferred from the shift register to the receiver buffer. Therefore, there is one full character time in which to read the character and decide whether or not it should be included in the CRC calculation. In the HDLC/SDLC mode, there is no 8-bit delay.

D4 **Enter hunt phase:** Although the MPSC receiver automatically enters the sync hunt phase after a reset, there are times when reentry may be desired, such as when it has been determined that synchronization has been lost or – in an HDLC/SDLC mode – to ignore the current incoming message. Writing a one into this bit at any time after initialization causes the MPSC to reenter the hunt phase.

D5 **Auto-enable:** Setting this bit to one causes the DCD and CTS inputs to act as enable inputs to the receiver and transmitter, respectively.

D7, D6 **Number of received bits per character:** This field specifies the number of data bits assembled to form each character. The value may be changed on the fly while a character is being assembled and, if the change is made before reaching the new number of bits, it will affect that character. Otherwise the new specifications have effect on the next character received.

Received bits per character

00	Receive 5 data bits/character
01	Receive 7 data bits/character
10	Receive 6 data bits/character
11	Receive 8 data bits/character

Write Register 4 (WR4)

D7	D6	D5	D4	D3	D2	D1	D0
Clock Rate		Sync Mode		Number of Stop Bits per Sync Mode		Parity Even/Odd	Parity Enable

D0 **Parity enable:** Setting this bit to one adds an extra data bit containing parity information to each transmitted character. Each received character is expected to contain this extra bit and the receiver parity checker is enabled.

D1 **Parity even/odd:** Programming a zero into this bit when parity is enabled causes the transmitted parity bit to take on the value required for odd parity. The received character is checked for odd parity. Conversely, a one in this bit signifies even parity generation and checking.

D3, D2 **Number of stop bits per sync mode:** This field specifies whether the channel is used in a synchronous (HDLC/SDLC) or an asynchronous mode. In an asynchronous mode this field also specifies the number of bit times used as the stop bit length by the transmitter. The receiver always checks for one stop bit.

Stop bits

00 Synchronous modes
01 Asynchronous 1-bit time (1 stop bit)
10 Asynchronous 1½ bit time (1½ stop bits)
11 Asynchronous 2-bit time (2 stop bits)

D5, D4 **Sync mode:** When the stop bits/sync mode field is programmed for synchronous modes (D2, D3 = 00), this field specifies the particular synchronous format to be used. This field is ignored in an asynchronous mode.

Synchronous formats

00 8-bit internal synchronization character (monosync)
01 16-bit internal synchronization character (bisync)
10 HDLC/SDLC
11 External synchronization (SYNC pin becomes an input)

D7, D6 **Clock rate:** This field specifies the relationship between the transmitter and receiver clock inputs ($\overline{TxC}$, $\overline{RxC}$) and the actual data rates at TxD and RxD. When operating in a synchronous mode a 1x clock rate must be specified. In asynchronous modes any of the rates may be specified, however, with a 1x clock rate the receiver cannot determine the center of the start bit. In this mode, the sampling (rising) edge of $\overline{RxC}$ must be externally synchronized with the data.

Clock rates

00 Clock rate = 1x data rate
01 Clock rate = 16x data rate
10 Clock rate = 32x data rate
11 Clock rate = 64x data rate

Write Register 5 (WR5)

D7	D6	D5	D4	D3	D2	D1	D0
DTR	Number of Bits Transmitted per Character		Send Break	Transmitter Enable	CRC Polynomial Select	$\overline{RTS}$	Transmitter CRC Enable

D0 **Transmitter CRC enable:** A one or a zero enables or disables respectively, the CRC generator calculation. The enable or disable does not take place until the next character is transferred from the transmitter buffer to the shift register, thus allowing specific characters to be included or excluded from the CRC calculation. By setting or resetting this bit just before loading the next character, this and subsequent characters are included or excluded from the calculation. If this bit is zero when the transmitter becomes empty, the MPSC goes to the idle phase regardless of the state of the idle/CRC latch.

D1 **$\overline{RTS}$:** In synchronous and HDLC/SDLC modes setting this bit to one causes the $\overline{RTS}$ pin to go low while a zero causes it to go high. In an asynchronous mode setting this bit to zero does not cause $\overline{RTS}$ to go high until the transmitter is completely empty. This feature facilitates programming the MPSC for use with asynchronous modems.

D2 **CRC polynomial select:** This bit selects the polynomial used by the transmitter and receiver for CRC generation and checking. A one selects the CRC 16 polynomial ($x^{16}+x^{15}+x^2+1$). A zero selects the CRC CCITT polynomial ($x^{16}+x^{12}+x^5+1$). In HDLC/SDLC mode, CRC CCITT must be selected. Either polynomial may be used in other synchronous modes.

D3 **Transmitter enable:** After a reset the transmitted data output (TxD) is held high (marking) and the transmitter is disabled until this bit is set. In an asynchronous mode TxD remains high until data is loaded for transmission.
In synchronous and HDLC/SDLC modes the MPSC automatically enters the idle phase and sends the programmed sync or flag characters.
When the transmitter is disabled in an asynchronous mode any character currently being sent is completed before TxD returns to the marking state.
If the transmitter is disabled during the data phase in a synchronous mode the current character is sent. TxD then goes high (marking). In HDLC/SDLC mode the current character is sent, but the marking line following is zero-inserted. That is, the line goes low for one bit time out of every five.
The transmitter should never be disabled during the HDLC/SDLC data phase unless a reset is to follow immediately. In either case, any character in the buffer register is held.
Disabling the transmitter during the CRC phase causes the remainder of the CRC character to be bit-substituted with the sync (or flag). The total number of bits transmitted is correct and TxD goes high after they are sent.
If the transmitter is disabled during the idle phase the remainder of the sync (flag) character is sent. TxD then goes high.

D4 **Send break:** Setting this bit to one immediately forces the transmitter output (TxD) low (spacing). This function overrides the normal transmitter output and destroys any data being transmitted although the transmitter is still in operation. Resetting this bit releases the transmitter output.

D6, D5 **Transmitted bits per character:** This field controls the number of data bits transmitted in each character. The number of bits per character may be changed by rewriting this field just before the first character is loaded to use the new specification.

Transmitted Bits per Character

Transmitted Bits per Character 1	Transmitted Bits per Character	
D6	D5	Bits per Character
0	0	5 or Less (see below)
0	1	7
1	0	6
1	1	8

Normally each character is sent to the MPSC right-justified and the unused bits are ignored. However, when sending five bits or less the data should be formatted as shown below to inform the MPSC about the precise number of bits to be sent.

Transmitted Bits per Character for 5 Bits or Less

D7	D6	D5	D4	D3	D2	D1	D0	Number of Bits per Character
1	1	1	1	0	0	0	D0	1
1	1	1	0	0	0	D1	D0	2
1	1	0	0	0	D2	D1	D0	3
1	0	0	0	D3	D2	D1	D0	4
0	0	0	D4	D3	D2	D1	D0	5

D7 **$\overline{\text{DTR}}$ (data terminal ready):** When this bit is one the $\overline{\text{DTR}}$ output is low (active). Conversely, when this bit is zero DTR is high.

Write Register 6 (WR6)

D7	D6	D5	D4	D3	D2	D1	D0
Sync Byte 1							

D7 to D0 Sync byte 1
Sync byte 1 is used in the following modes:
Monosync 8-bit sync character transmitted during the idle phase.
Bisync Least significant (first) 8 bits of the 16-bit transmit and receive sync character.
External sync Sync character transmitted during the idle phase.
HDLC/SDLC Secondary address value matched to secondary address field of the HDLC/SDLC frame when the MPSC is in the address search mode.

Write Register 7 (WR7)

D7	D6	D5	D4	D3	D2	D1	D0
Sync Byte 2							

D7 to D0 Sync byte 2
Sync byte 2 is used in the following modes:
Monosync 8-bit sync character matched by the receiver.
Bisync Most significant (second) 8 bits of the 16-bit transmit and receive sync characters.
HDLC/SDLC The flag character, 0111 1110, must be programmed into control register 7 for flag matching by the MPSC receiver.

Read Register 0 (RR0)

D7	D6	D5	D4	D3	D2	D1	D0
Break/ Abort	Tx Underrun /EOM	CTS	Sync Status	DCD	Transmitter Buffer Empty	Interrupt Pending	Received Character Available

D0 **Received character available:** When this bit is set it indicates that one or more characters in the receiver buffer are available for the processor to read. Once all the available characters have been read the MPSC resets this bit until a new character is received.

D1 **Interrupt pending (channel A only):** The interrupt pending bit is used with the interrupt vector register (read register 2) to make it easier to determine the MPSC's interrupt status, particularly in a nonvectored interrupt mode where the processor must poll each device to determine the interrupt source. In this mode interrupt pending is set when read register is read, the $\overline{PRI}$ input is active (low), and the MPSC is requesting interrupt service.
The status registers of both channels need not be analyzed to determine if an interrupt is pending. If the status-affects-vector is enabled and the interrupt pending is set, the vector read from RR2 contains valid condition information.

In a vectored interrupt mode, interrupt pending is set during the interrupt acknowledge cycle (on the leading edge of the second $\overline{INTA}$ pulse) when the MPSC is the highest priority device requesting interrupt service ($\overline{PRI}$ is active). In either mode, if there are no other pending interrupt requests, interrupt pending is reset when the end of the interrupt command is issued.

D2 **Transmitter buffer empty:** This bit is set whenever the transmitter buffer is empty except during the transmission of CRC. (The MPSC uses the buffer to facilitate this function.) After a reset the buffer is considered empty and transmit buffer empty is set.

D7 to D3 **External/status flags:** The following status bits reflect the state of the various conditions that cause an external/status interrupt. The MPSC latches all external/status bits whenever a change occurs that would cause an external/status interrupt (regardless of whether this interrupt is enabled). This allows transient status changes on these lines to be captured with relaxed software timing requirements.
When the MPSC is operated in an interrupt-driven mode for external/status interrupts, read register 0 should be read when this interrupt occurs and a "reset external/status interrupt" command issued to reenable the interrupt and the latches. To poll these bits without interrupts, the "reset external/status interrupt" command can be issued to first update the status to reflect the current values.

D3 **$\overline{DCD}$:** This bit reflects the inverted state of the $\overline{DCD}$ input. When $\overline{DCD}$ is low the DCD status bit is high. Any transition on this bit causes an external/status interrupt request.

D4 **Sync status:** The meaning of this bit depends on the operating mode of the MPSC.

Asynchronous mode: Sync status reflects the inverted state of the $\overline{SYNC}$ input. When $\overline{SYNC}$ is low, sync status is high. Any transition on this bit causes an external/status interrupt request.

External synchronization mode: Sync status operates in the same manner as in asynchronous mode. The MPSC's receiver synchronization logic is also tied to the sync status bit in external synchronization mode and a low-to-high transition ($\overline{SYNC}$ input going low) informs the receiver that synchronization has been achieved and character assembly begins.
A low-to-high transition on the $\overline{SYNC}$ input indicates that synchronization has been lost and is reflected both in the sync status becoming zero and the generation of an external/status interrupt. The receiver remains in the receive data phase until the enter hunt phase bit in write register 3 is set.

Monosync, bisync, HDLC/SDLC modes: In these modes, sync status indicates whether the MPSC receiver is in the sync hunt or receive data phase of operation. A zero indicates that the MPSC is in the receive data phase and a one indicates that the MPSC is in the sync hunt phase (as after a reset or a setting of the enter sync hunt phase bit). Like in the other modes a transition on this bit causes an external/status interrupt to be issued. It should be noted that entering a sync hunt phase after either a reset or when programmed causes an external/status interrupt request which may be cleared immediately with a "reset external/ status interrupt" command.

D5 **CTS:** This bit reflects the inverted state of the $\overline{CTS}$ input. When $\overline{CTS}$ is low, the CTS status bit is high. Any transition on this bit causes an external/status interrupt request.

D6 **Tx underrun/EOM:** This bit indicates the state of the Tx underrun/EOM latch used in the synchronous and HDLC/SDLC modes. After a hardware reset this bit is set to one, indicating that the transmitter is completely empty. When the MPSC enters idle phase it automatically transmits sync or flag characters. In the HDLC/SDLC mode the MPSC automatically resets this latch after the first byte of a frame is written to the Tx buffer. When the transmitter is completely empty, the MPSC sends the 16-bit CRC character and sets the latch again. An external/status interrupt is issued when the latch is set, indicating that CRC is being sent. No interrupt is issued when the latch is reset.

Break/abort: In the asynchronous mode this bit indicates the detection of a break sequence (a null character plus framing error that occurs when the RxD input is held low, spacing, for more than one character time). Break/abort is reset when RxD returns high (marking).
In the HDLC/SDLC mode, break/abort indicates the detection of an abort sequence when seven or more ones are received in sequence. It is reset when a zero is received.
Any transition of the break/abort bit causes an external/status interrupt.

Read Register 1 (RR1)

D7	D6	D5	D4	D3	D2	D1	D0
End of HDLC/ SDLC Frame	CRC Framing Error	Overrun Error	Parity Error	HDLC/SDLC Residue Code			All Sent

D0 **All sent:** This bit is set when the transmitter is empty and reset when a character is present in the transmitter buffer or shift register. This feature simplifies the modem control software routines. In the bit-synchronous mode, this bit will be set when the ending flag pattern is sent.

D3 to D1 **HDLC/SDLC residue code:** Since the data portion of an HDLC/SDLC message can consist of any number of bits and not necessarily an integral number of characters, the MPSC features special logic to determine and report when the end of frame flag has been received, the boundary between the data field and the CRC character in the last few data characters that were just read.

When the end of frame condition is indicated, that is, read register 1D7 = 1 and special receive condition interrupt (if enabled), the last bits of the CRC character are in the receiver buffer. The residue code for the frame is valid in the read register 1 byte associated with that data character (RR1 tracks the received data in its own buffer).
The meaning of the residue code depends upon the number of bits per character specified for the receiver. The previous character refers to the last character read before the end of frame, and so forth.

Residue Codes

8 Bits per Character

D_3	D_2	D_1	Previous Character	2nd Previous Character	
1	0	0	C C C C C C C C	C C C C C D D D	
0	1	0	C C C C C C C C	C C C C D D D D	
1	1	0	C C C C C C C C	C C C D D D D D	
0	0	1	C C C C C C C C	C C D D D D D D	
1	0	1	C C C C C C C C	C D D D D D D D	
0	1	1	C C C C C C C C	D D D D D D D D	(no residue)
1	1	1	C C C C C C C D	D D D D D D D D	
0	0	0	C C C C C C D D	D D D D D D D D	

7 Bits per Character

D_3	D_2	D_1	Previous Character	2nd Previous Character	
1	0	0	C C C C C C C	C C C C C D D	
0	1	0	C C C C C C C	C C C C D D D	
1	1	0	C C C C C C C	C C C D D D D	
0	0	1	C C C C C C C	C C D D D D D	
1	0	1	C C C C C C C	C D D D D D D	
0	1	1	C C C C C C C	D D D D D D D	(no residue)
0	0	0	C C C C C C D	D D D D D D D	

6 Bits per Character

D_3	D_2	D_1	Previous Character	2nd Previous Character	
1	0	0	C C C C C C	C C C C C D	
0	1	0	C C C C C C	C C C C D D	
1	1	0	C C C C C C	C C C D D D	
0	0	1	C C C C C C	C C D D D D	
1	0	1	C C C C C C	C D D D D D	
0	0	0	C C C C C C	D D D D D D	(no residue)

5 Bits per Character

D_3	D_2	D_1	2nd Previous Character	3rd Previous Character	
1	0	0	C C C C C	D D D D D	(no residue)
0	1	0	C C C C D	D D D D D	
1	1	0	C C C D D	D D D D D	
0	0	1	C C D D D	D D D D D	
0	0	0	C D D D D	D D D D D	

Special receive condition flags

The status bits described in the following – parity error (if parity as a special receive condition is enabled), receiver overrun error CRC/framing error, and end of HDLC/SDLC frame – all represent special receive conditions.

When any of these conditions occur and interrupts are enabled, the MPSC issues an interrupt request. In addition, if a condition-affects-vector mode is enabled, the vector generated (and the contents of RR2B for nonvectored interrupts) is different from that of a received-character-available condition. Thus, it is not necessary to analyze RR1 with each character to determine if an error has occurred.

As a further convenience, the parity error and receiver overrun error flags are latched. That is, once one of these errors occurs, the flag remains set for all subsequent characters until reset by the error reset command. With this facility RR1 need only be read at the end of a message to determine if either of these errors occurred anywhere in the message. The other flags are not latched and follow each character available in the receiver buffer.

D4 **Parity error:** This bit is set and latched when parity is enabled and the received parity bit does not match the sense (odd or even) calculated from the data bits.

D5 **Receiver overrun error:** This error occurs and is latched when the receiver buffer already contains three characters and a fourth character is completely received, overwriting the last character in the buffer.

D6 **CRC/framing error:** In the asynchronous mode a framing error is flagged (but not latched) when no stop bit is detected at the end of a character (i.e. RxD is low one bit time after the center of the last data or parity bit). When this condition occurs, the MPSC waits an additional one-half bit time before sampling again so that the framing error is not interpreted as a new start bit.
In the synchronous and HDLC/SDLC modes this bit indicates the result of the comparison between the current CRC result and the appropriate check value and is usually set to one since a message rarely indicates a correct CRC result until correctly completed with the CRC check character. Note that a CRC error does not result in a special receive condition interrupt.

D7 **End of HDLC/SDLC frame (EOF):** This status bit is used only in the bit synchronous mode to indicate that the end of frame flag has been received and that the CRC error flag and residue code are valid. This flag can be reset at any time by issuing an error reset command. The MPSC also automatically resets this bit when the first character of the next message frame is sent.

Read Register 2B (RR2B)

D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Vector							

D7 to D0 **Interrupt vector (channel B only):** Reading read register 2B returns the interrupt vector that is programmed into write register 2B. If a condition-affects-vector mode is enabled the value of the vector is modified as shown in the following table.

Status-Affects-Vector Modifications

Interrupt Pending (RR0, D1 Channel A)	8085 Modes / 8086 Modes	D4 / D2	D3 / D1	D2 / D0	Condition
0		1	1	1	No Interrupt Pending
1		0	0	0	Channel B Transmitter Buffer Empty
1		0	0	1	Channel B External/Status Change
1		0	1	0	Channel B Received Character Available
1		0	1	1	Channel B Special Receive Condition
1		1	0	0	Channel A Transmitter Buffer Empty
1		1	0	1	Channel A External/Status Change
1		1	1	0	Channel A Received Character Available
1		1	1	1	Channel A Special Receive Condition

As can be seen code 111 can mean either channel A special receive condition or no interrupt pending. They can be easily distinguished by examining the interrupt pending bit (D1) of read register 0, channel A. In a nonvectored interrupt mode the vector register must be read first for the interrupt pending to be valid.

Read Registers 3 and 4 (RR3, RR4)
Tx Byte Counter (low byte RR3, high byte RR4)

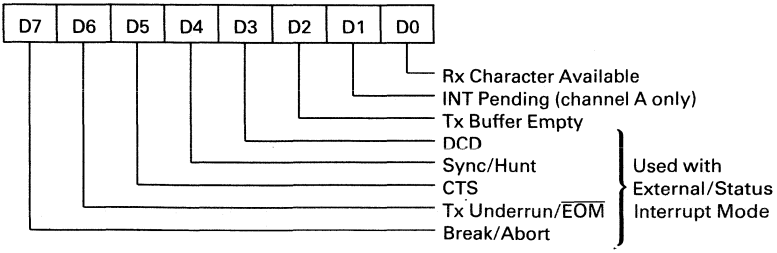
D7	D6	D5	D4	D3	D2	D1	D0
Tx Byte Counter (low byte)							

D7	D6	D5	D4	D3	D2	D1	D0
Tx Byte Counter (high byte)							

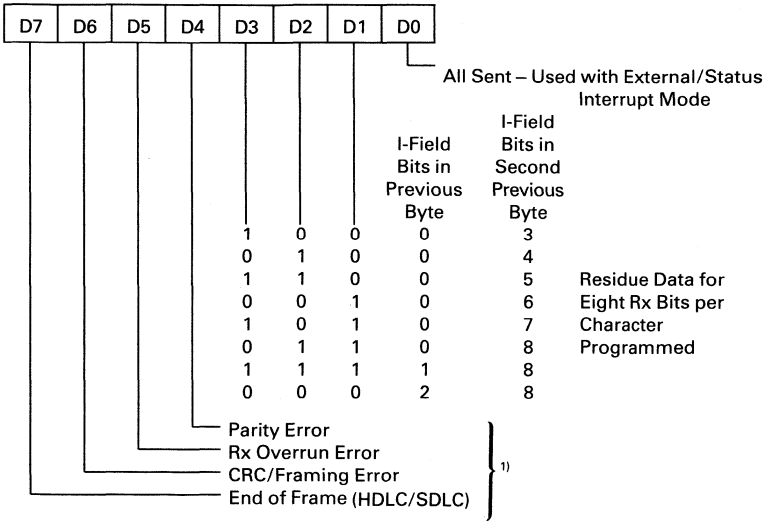
These two registers are used to count the number of transmit data. They can be used when data transmission is performed in the Tx byte count enable mode (i.e., when bit D6 of WR1 is 1). The values of the counters are cleared when the system is reset, when the contents of the Tx length registers (addressed via WR1) coincide with those of RR3, RR4 or when Tx length registers are set by setting bit D6 of the WR1 to 1.

Read Register Bit Functions

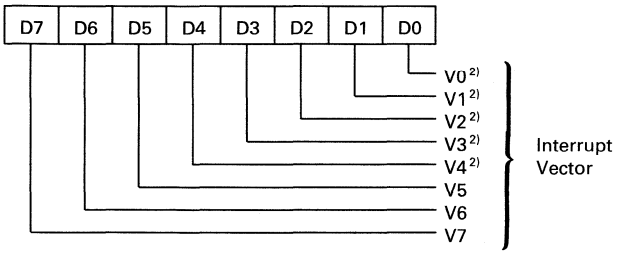
Read register 0



Read register 1

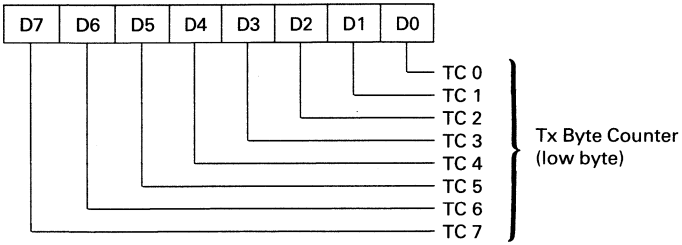


Read register 2 (channel B only)

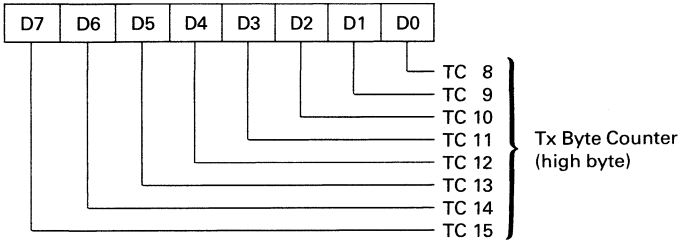


1) Used with special receive condition mode.
2) Variable if status-affects-vector is programmed.

Read register 3

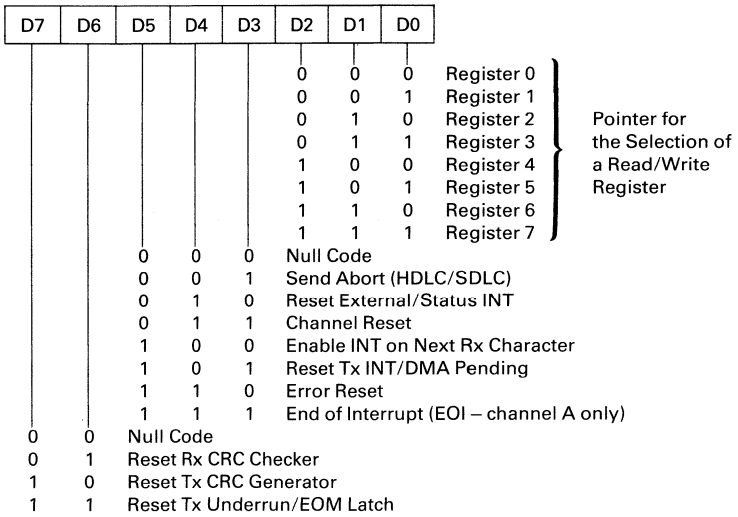


Read register 4

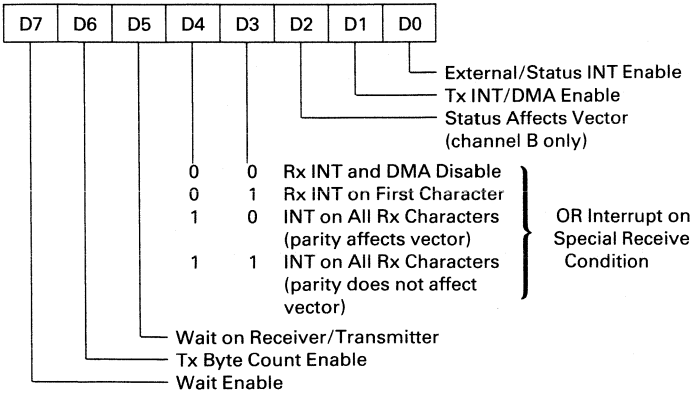


Write Register Bit Functions

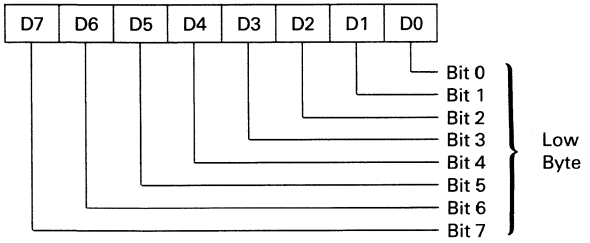
Write register 0



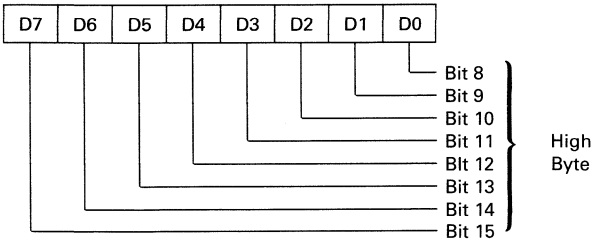
Write register 1



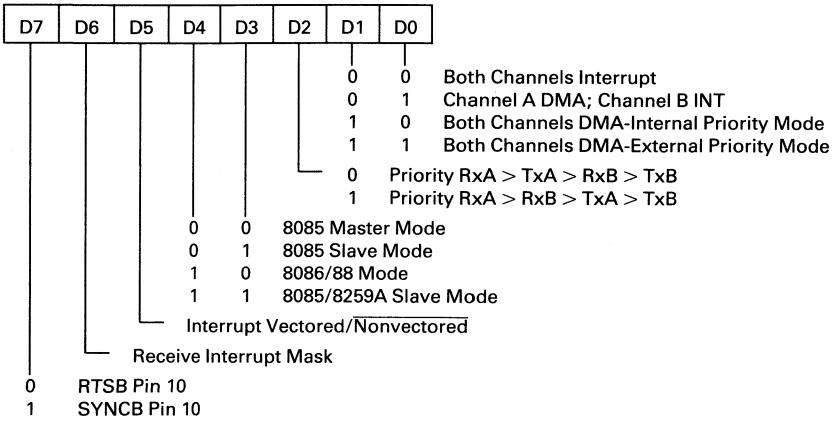
Tx length register



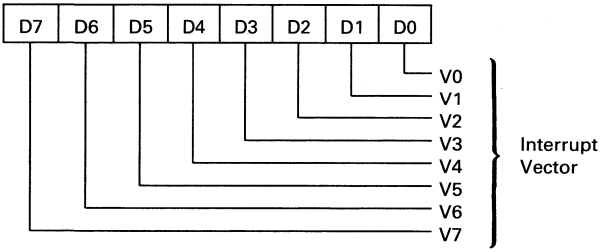
Tx length register



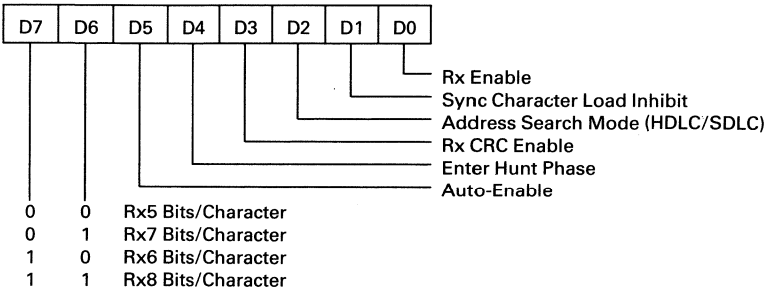
Write register 2 (channel A)



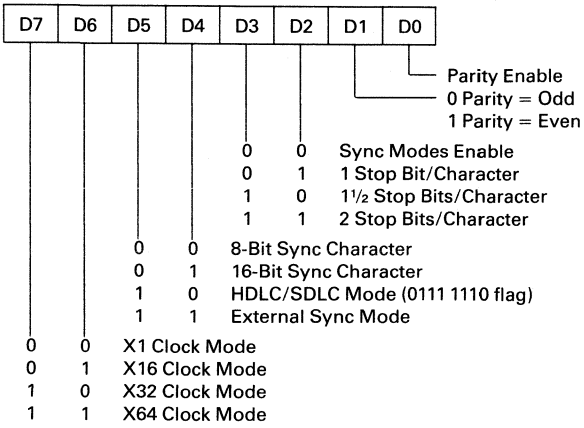
Write register 2 (channel B)



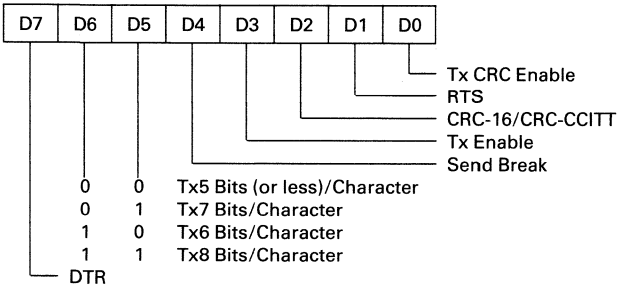
Write register 3



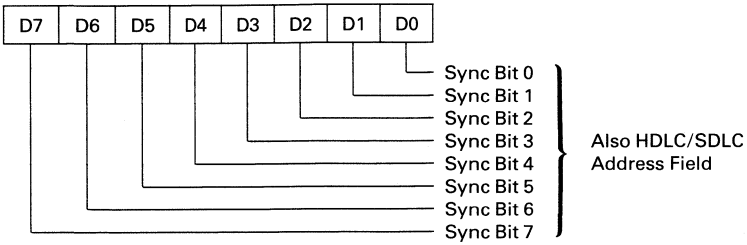
Write register 4



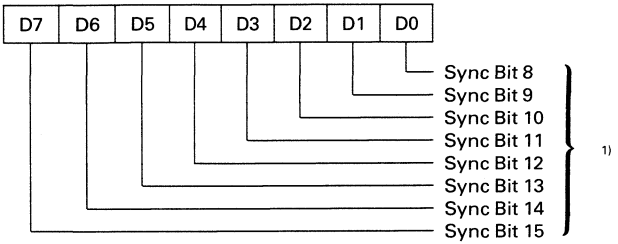
Write register 5



Write register 6



Write register 7



[1] For HDLC/SDLC it must be programmed to 0111 1110 for flag recognition.

Absolute Maximum Ratings [1)]

Temperature under bias	0 to + 70°C
Storage temperature	−65 to +150°C
All output and supply voltages	−0.5 to + 7V
All input voltages	−0.5 to + 7V
Power dissipation	1.0W

DC Characteristics

(TA = 0 to 70°C, VCC = 5V ±10%)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC+0.5V	V	–
VOL	Output low voltage	–	0.45	V	IOL = 2.0 mA
VOH	Output high voltage	2.4	–	V	IOH = −200 µA
IIL	Input load current	–	±10	µA	VIN = VCC to 0V
IOFL	Output float leakage	–	±10	µA	VOUT = VCC to 0V
ICC	VCC supply current	–	200	mA	–

Capacitance

(TA = 25°C, VCC = GND = 0V)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
CIN	Input capacitance	–	10	pF	fc = 1 MHz
COUT	Output capacitance	–	15	pF	Unmeasured pins returned to GND
CIO	I/O capacitance	–	20	pF	

[1)] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

(TA = 0 to 70°C, VCC = +5V ±10%)

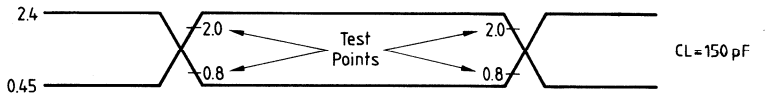
Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCY	Clock cycle	200	4000	ns	–
TCH	Clock pulse width high	70	2000	ns	–
TCL	Clock pulse width low	70	2000	ns	–
TR	Clock rise time	0	30	ns	–
TF	Clock fall time	0	30	ns	–
TAR	Address setup time to $\overline{RD}$	0	–	ns	–
TRA	Address hold time from $\overline{RD}$	0	–	ns	–
TRR	$\overline{RD}$ pulse width	200	–	ns	–
TAD	Data output delay from address	–	200	ns	–
TRD	Data output delay from $\overline{RD}$	–	200	ns	–
TDF	Data float delay from $\overline{RD}$	10	100	ns	–
TAW	Address setup time to $\overline{WR}$	0	–	ns	–
TWA	Address hold time from $\overline{WR}$	0	–	ns	–
TWW	$\overline{WR}$ pulse width	200	–	ns	–
TDW	Data setup time to $\overline{WR}$	130	–	ns	–
TWD	Data hold time from $\overline{WR}$	0	–	ns	–
TPIPO	$\overline{PRO}$ delay time from $\overline{PRI}$	–	100	ns	–
TIAPO	$\overline{PRO}$ delay time from $\overline{INTA}$	–	200	ns	–
TPIIA	$\overline{PRI}$ setup time to $\overline{INTA}$	0	–	ns	–
TIAPI	$\overline{PRI}$ hold time from $\overline{INTA}$	20	–	ns	–
TIAIA	$\overline{INTA}$ pulse width	200	–	ns	–
TIAD	Data output delay from $\overline{INTA}$	–	200	ns	–
TDF	Data float delay from $\overline{INTA}$	10	100	ns	–
TCQ	DRQ hold time from $\overline{RD}$, $\overline{WR}$	–	150	ns	–
THIC	$\overline{HAI}$ setup time to $\overline{RD}$, $\overline{WR}$	300	–	ns	–
TCHI	$\overline{HAI}$ hold time from $\overline{RD}$, $\overline{WR}$	0	–	ns	–
THIHO	$\overline{HAO}$ delay time from $\overline{HAI}$	–	100	ns	–
TDCY	Data clock cycle	400	–	ns	$\overline{RxC}$, $\overline{TxC}$
TDCH	Data clock pulse width high	180	–	ns	$\overline{RxC}$, $\overline{TxC}$
TDCL	Data clock pulse width low	180	–	ns	$\overline{RxC}$, $\overline{TxC}$

AC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TTCTD	Tx data delay time from TxC	–	300	ns	x1 mode
		–	1000	ns	x16, x32, x64 mode
TRDRC	Rx data setup time to $\overline{RxC}$	0	–	ns	–
TRCRD	Rx data hold time from $\overline{RxC}$	140	–	ns	–
TTDI	$\overline{INT}$ delay time from Tx data	–	4–6	TCY	–
TRCI	$\overline{INT}$ delay time from $\overline{RxC}$	–	7–11	TCY	–
TMH	$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse width high	200	–	ns	–
TML	$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse width low	200	–	ns	–
TMI	$\overline{INT}$ delay from $\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$	–	500	ns	–
TRV	Recovery time for $\overline{RD}$, $\overline{WR}$	300	–	ns	–
TAWT	$\overline{WAIT}$ delay time from address	–	120	ns	–
TRCS	$\overline{SYNC}$ setup time to $\overline{RxC}$	–	100	ns	–

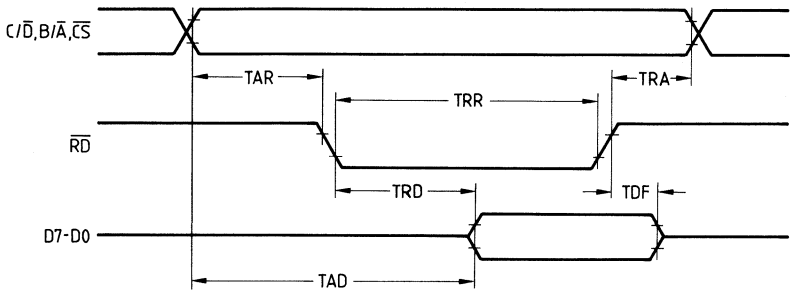
Note
$\overline{RESET}$ must be active for a minimum of one complete CLK cycle.
In all modes, system clock rate must be 4.5 times data rate.

AC Testing Input/Output Waveform

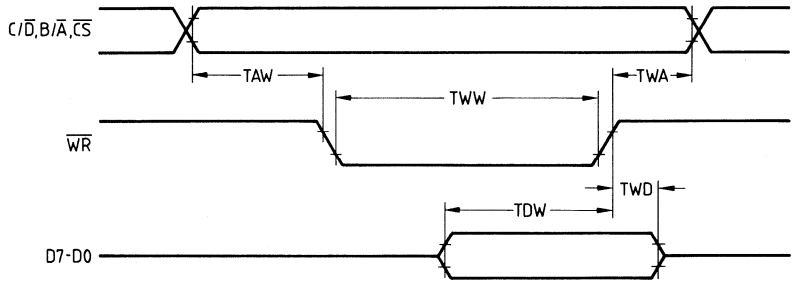


Waveforms

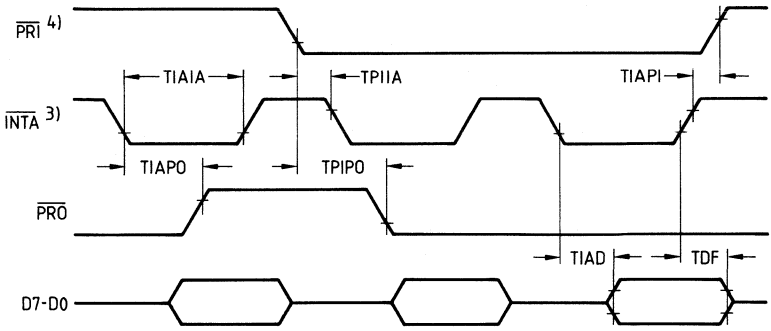
Read Cycle Timing



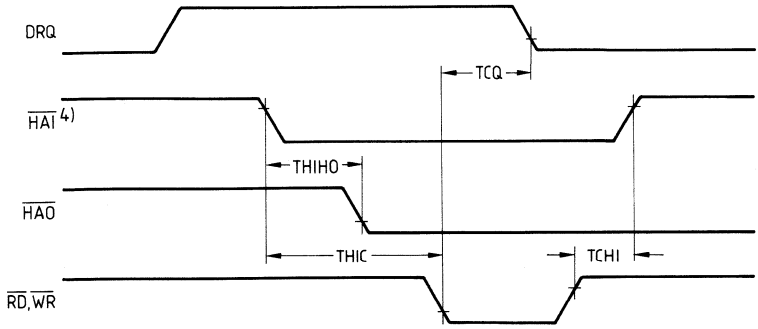
Write Cycle Timing



$\overline{\text{INTA}}$ Cycle Timing

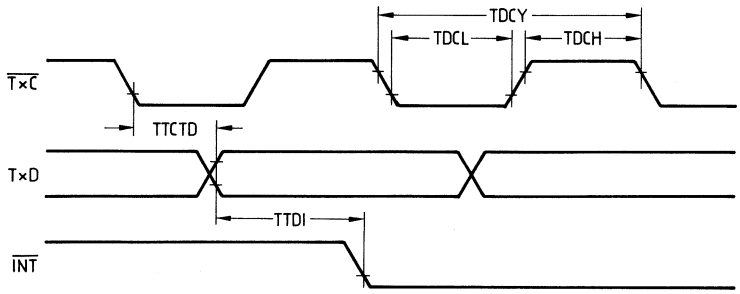


DMA Cycle Timing

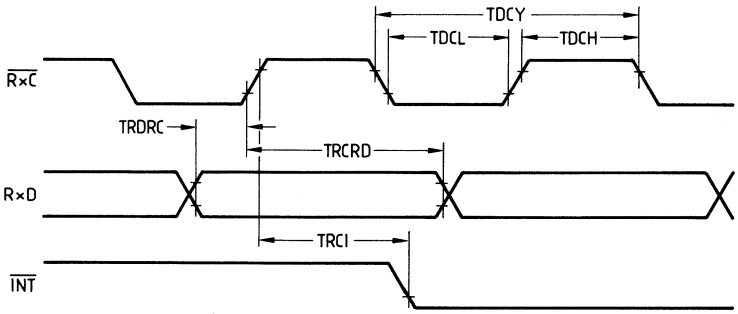


Note
3) $\overline{\text{INTA}}$ signal acts as $\overline{\text{RD}}$ signal.
4) $\overline{\text{PRI}}$ and $\overline{\text{HAI}}$ signals act as $\overline{\text{CS}}$ signal.

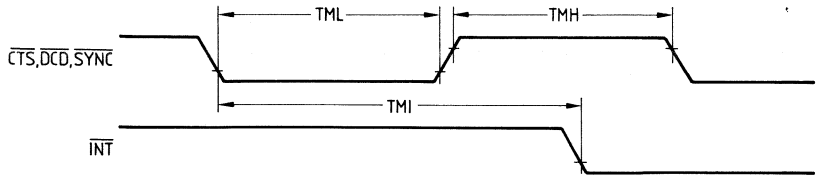
Transmit Cycle Timing



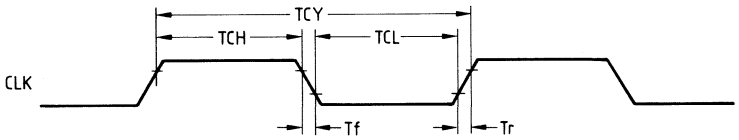
Receive Cycle Timing



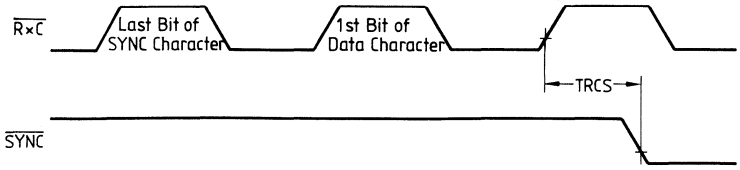
External/Status Timing



Clock Timing

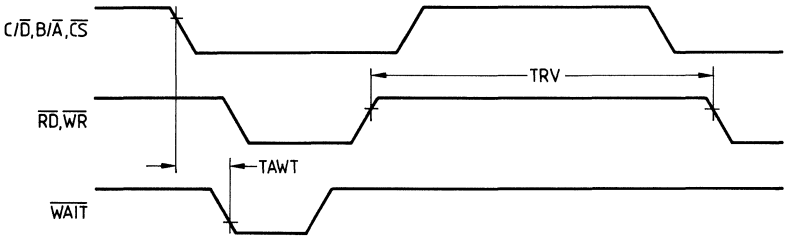


$\overline{\text{SYNC}}$ Input Timing (external sync mode)



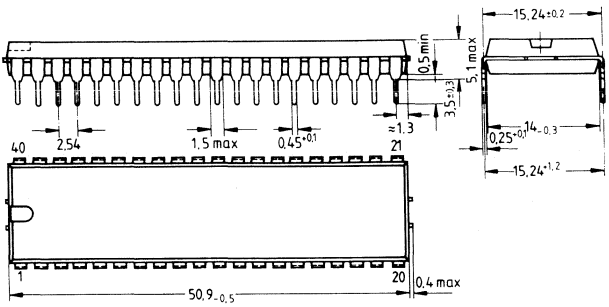
$\overline{\text{SYNC}}$ input should become 0 (low level) at rising edge of $\overline{\text{RxC}}$ after two clock cycles from the last bit of SYNC character.

Read/Write Cycle Timing (software block transfer mode)



Package Outline

40-Pin Plastic Package, Type P



Dimensions in mm

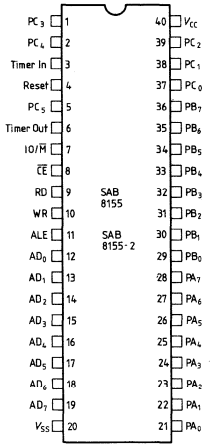
Ordering Information

Type	Description	Ordering code
SAB 7201A-P	Multi-protocol serial communication controller MPSC	Q67120-P143

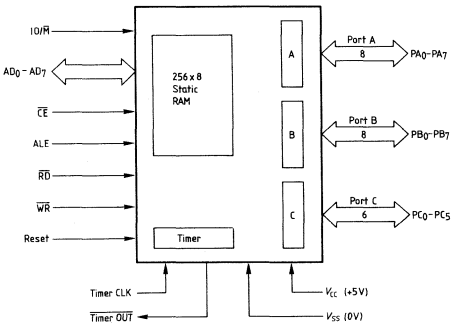
SAB 8155, 8155-2
2048 Bit Static MOS RAM with I/O Ports and Timer

- 256 Word × 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8-Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with SAB 8085A and SAB 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

Pin Configuration



Block Diagram



The SAB 8155 is a RAM and I/O chip to be used in the SAB 8085A and SAB 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256×8. They have a maximum access time of 400ns to permit use with no wait states in SAB 8085A CPU. The SAB 8155-2 has a maximum access time of 330ns for use with the SAB 8085A-2 and the full speed 5MHz SAB 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

5.82

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
PCØ–PC5	1, 2, 5, 37–39	I/O	PORT C – These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PCØ-PC5 are used as control signals, they will provide the following: PCØ – A INTR (Port A Interrupt) PC1 – ABF (Port A Buffer Full) PC2 – $\overline{\text{A STB}}$ (Port A Strobe) PC3 – B INTR (Port B Interrupt) PC4 – B BF (Port B Buffer Full) PC5 – $\overline{\text{B STB}}$ (Port B Strobe)
TIMER IN	3	I	TIMER INPUT – Input to the counter/timer.
RESET	4	I	RESET – Pulse provided by the SAB 8085A to initialize the system (connect to SAB 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports in input mode. The width of RESET pulse should typically be two SAB 8085A clock cycle times.
$\overline{\text{TIMER OUT}}$	6	O	TIMER OUTPUT – This output can be either a square wave or a pulse, depending on the timer mode.
IO/$\overline{\text{M}}$	7	I	I/O MEMORY – Selects memory if low and I/O and command/status registers if high.
$\overline{\text{CE}}$	8	I	CHIP ENABLE – On this SAB 8155, this pin is $\overline{\text{CE}}$ and is ACTIVE LOW.
$\overline{\text{RD}}$	9	I	READ CONTROL – Input low on this line with the Chip Enable active enables and ADØ–AD7 buffers. If IO/$\overline{\text{M}}$ pin is low, the RAM contents will be read out to the AD bus. Otherwise the contents of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{\text{WR}}$	10	I	WRITE CONTROL – Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{\text{M}}$.
ALE	11	I	ADDRESS LATCH ENABLE – This control signal latches both the address on the ADØ–AD7 lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
ADØ–AD7	12–19	I/O	ADDRESS/DATA – 3-state Address/Data lines that interface with the CPU lower 8-bit Address-Data Bus. The 8-bit address is latched into the address latch inside the SAB 8155 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{\text{M}}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{\text{WR}}$ or $\overline{\text{RD}}$ input signal.

Symbol	Number	Input (I) Output (O)	Function
PAØ–PA7	21–28	I/O	PORT A – These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PBØ–PB7	29–36	I/O	PORT B – These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
V_{CC}	40		POWER SUPPLY (+5V)
V_{SS}	20		GROUND (0 V)

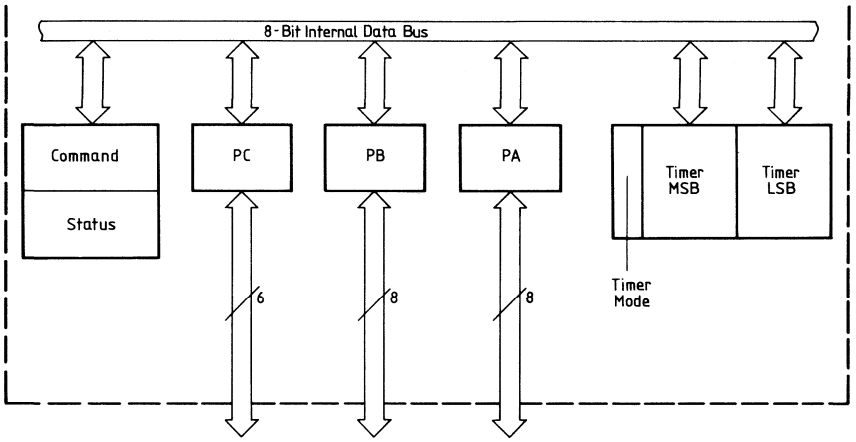
Functional Description

The SAB 8155 contains the following:

- 2Kbit Static RAM organized as 256×8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA∅–PA7, PB∅–PB7, PC∅–PC5) or the memory (RAM) portion.

SAB 8155 Internal Registers



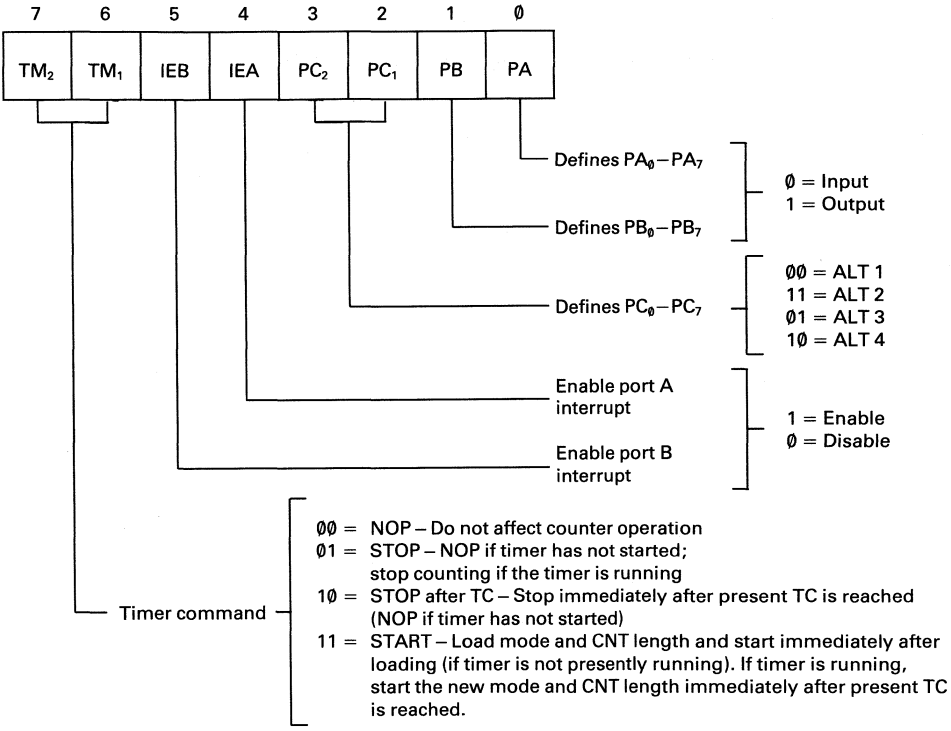
The 8-bit address on the Address/Data lines, Chip Enable input $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

Programming of the Command Register

The command register consists of eight latches. Four bits (Ø–3) define the mode of the ports, two bits (4–5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6–7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXXØØØ during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in the following figure. The contents of the command register may never be read.

Command Register Bit Assignment

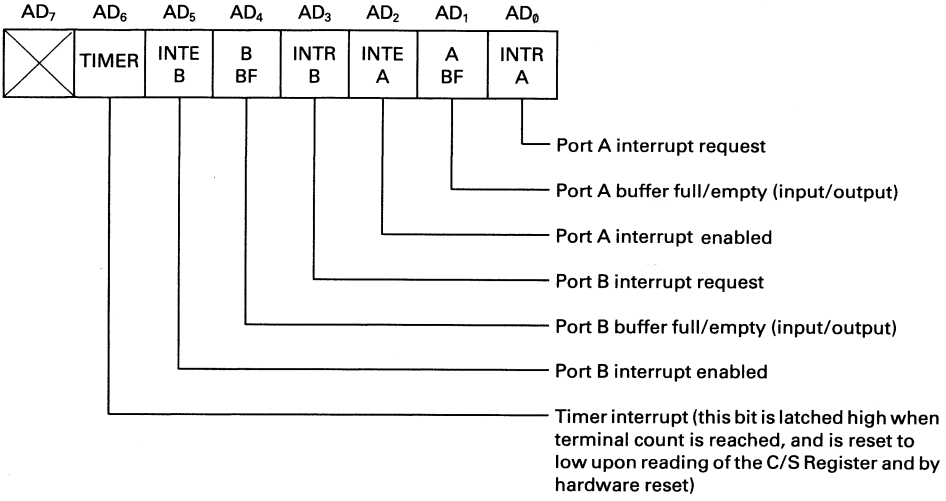


Reading the Status Register

The status register consists of seven latches, one for each bit; six (Ø–5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXXØØØ). Status word format is shown in the following figure. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

Status Register Bit Assignment



Input/Output Section

The I/O section of the SAB 8155 consists of five registers (see following figure):

- **Command/Status Register (C/S)** – Both registers are assigned the address XXXXXØØØ. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are **not** accessible through the pins.

  When the C/S (XXXXXØØØ) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the ADØ–AD7 lines.

- **PA Register** – This register can be programmed to be either input or – output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are PAØ–PA7. The address of this register is XXXXXØØ1.

- **PB Register** – This register functions the same as PA Register. The I/O pins assigned are PBØ–PB7. The address of this register is XXXXXØ1Ø.

- **PC Register** – This register has the address XXXXXØ11 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA und PB by properly programming the AD2 and AD3 bits of the C/S register.

  When PCØ–PC5 is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the SAB 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode (see table Port Control Assignment).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

Control	Input Mode	Output Mode
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

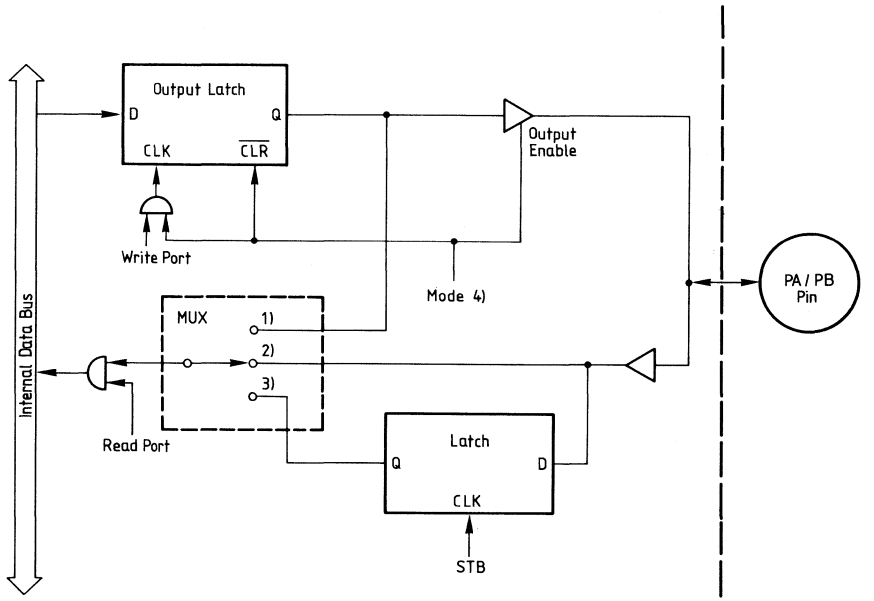
I/O Port and Timer Addressing Scheme

I/O Address *								Selection
A7	A6	A5	A4	A3	A2	A1	AØ	
X	X	X	X	X	Ø	Ø	Ø	Interval Command/Status Register
X	X	X	X	X	Ø	Ø	1	General Purpose I/O Port A
X	X	X	X	X	Ø	1	Ø	General Purpose I/O Port B
X	X	X	X	X	Ø	1	1	Port C – General Purpose I/O or Control
X	X	X	X	X	1	Ø	Ø	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	Ø	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care.
*: I/O Address must be qualified by $\overline{CE}$ = Ø and IO/$\overline{M}$ = 1 in order to select the appropriate register.

The following figure shows how I/O PORTS A and B are structured within the SAB 8155:

SAB 8155 Port Functions



Notes:
1) Output Mode
2) Simple Input
3) Strobed Input

} Multiplexer Control

4) = 1 for Output Mode
= Ø for Input Mode

Read Port = (IO/$\overline{M}$ = 1) × ($\overline{RD}$ = Ø) × (CE Active) × (Port Address selected)
Write Port = (IO/$\overline{M}$ = 1) × ($\overline{WR}$ = Ø) × (CE Active) × (Port Address selected)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the SAB 8155 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the SAB 8155 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

Port Control Assignment

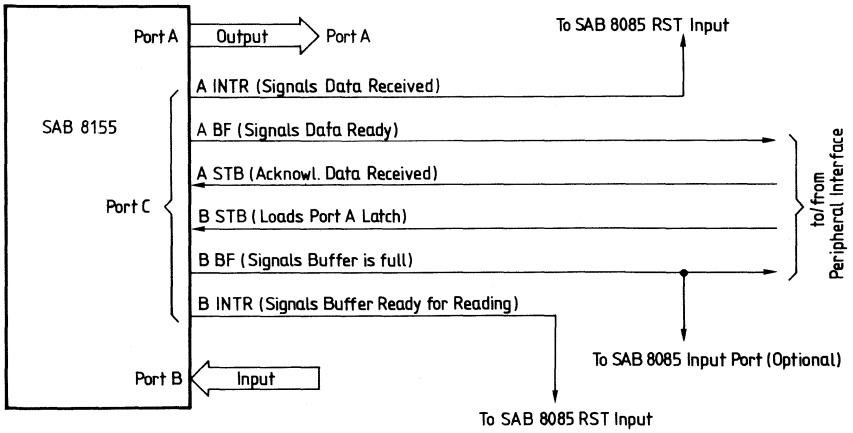
Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC∅	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{\text{STB}}$ (Port A Strobe)	A $\overline{\text{STB}}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{\text{STB}}$ (Port B Strobe)

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Next figure shows how the SAB 8155 I/O ports might be configured in a typical SAB 8085 system.

Example: Command Register = ∅∅111∅∅1



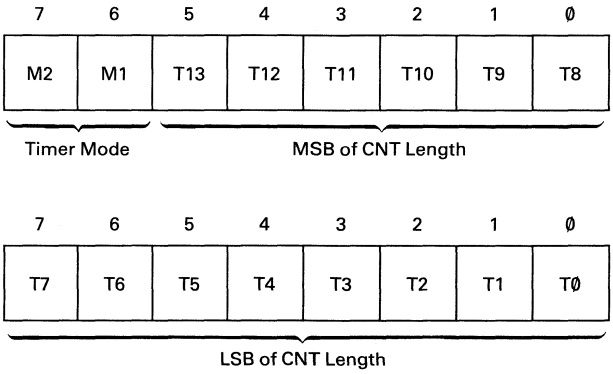
Timer Section

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register (see figure I/O Port and Timer Addressing Scheme).

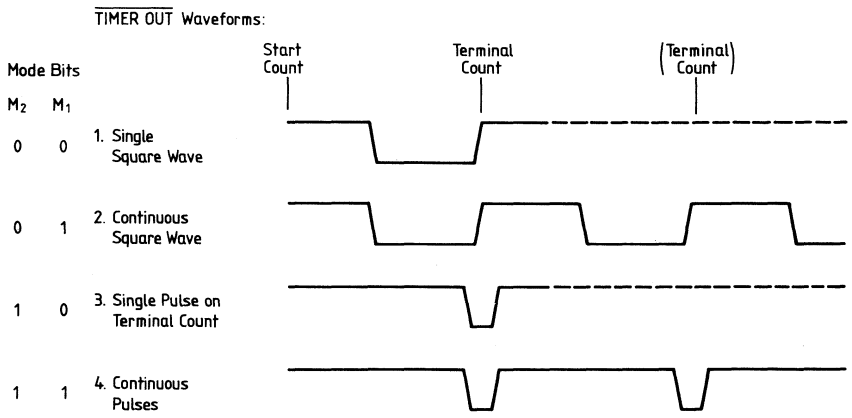
To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0–13 of the high order count register will specify the length of the next count and bits 14–15 of the high order register will specify the timer output mode (see next figure). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0–13.

Timer Format



There are four modes to choose from: M2 and M1 define the timer mode, as shown in following figure.

Timer Modes



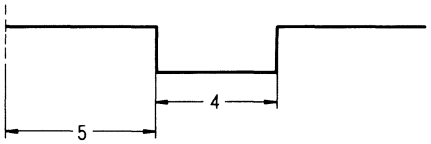
Bits 6–7 (TM2 and TM1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM2	TM1	Function
Ø	Ø	NOP – Do not affect counter operation
Ø	1	STOP – NOP if timer has not startet; stop counting if the timer is running
1	Ø	STOP AFTER TC – Stop immediately after present TC is reached (NOP if timer has not startet)
1	1	START – Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you **must** issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in next figure.

Asymmetrical Square-Wave Output Resulting from Count of 9



Note: 5 and 4 refer to the number of clocks in that time period

The counter in the SAB 8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the SAB 8155 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the SAB 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To abtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set. add ½ of the full original count (½ full count – 1 if full count is odd)

Note:
If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts have occured. Regardless of this, the SAB 8155 always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

Absolute maximum ratings *)

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
Voltage on any Pin with Respect to Ground	−0.5 to +7 V
Power Dissipation	1.5 Watt

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±5%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{IL}	Input Leakage	–	±10	µA	V_{IN} = V_{CC} to 0 V
I_{LO}	Output Leakage				0.45 V ≦ V_{OUT} ≦ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	–
I_{IL} (CE)	Chip Enable Leakage		+100	µA	V_{IN} = V_{CC} to 0 V

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

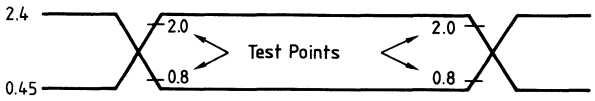
A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 5%

Symbol	Parameter	Limit Values				Units
		SAB 8155		SAB 8155-2		
		Min.	Max.	Min.	Max.	
t_{AL}	Address to Latch Set Up Time	50				
t_{LA}	Address Hold Time after Latch	80	–	30	–	
t_{LC}	Latch to READ/WRITE Control	100		40		
t_{RD}	Valid Data Out Delay from READ Control	–	170	–	140	
t_{AD}	Address Stable to Data Out Valid		400		330	
t_{LL}	Latch Enable Width	100	–	70	–	
t_{RDF}	Data Bus Float After READ	0	100	0	80	
t_{CL}	READ/WRITE Control to Latch Enable	20		10		
t_{CC}	READ/WRITE Control Width	250		200		
t_{DW}	Data In to WRITE Set Up Time	150	–	100	–	
t_{WD}	Data In Hold Time After WRITE	0		0		
t_{RV}	Recovery Time Between Controls	300		200		
t_{WP}	WRITE to Port Output	–	400	–	300	ns
t_{PR}	Port Input Setup Time	70	–	50	–	
t_{RP}	Port Input Hold Time	50	–	10	–	
t_{SBF}	Strobe to Buffer Full	–	400	–	300	
t_{SS}	Strobe Width	200	–	150	–	
t_{RBE}	READ to Buffer Empty					
t_{SI}	Strobe to INTR ON	–	400	–	300	
t_{RDI}	READ to INTR Off					
t_{PSS}	Port Setup Time to Strobe Strobe	50	–	0	–	
t_{PHS}	Port Hold Time After Strobe	120		100		
t_{SBE}	Strobe to Buffer Empty					
t_{WBF}	WRITE to Buffer Full					
t_{WI}	WRITE to INTR Off	–	400	–	300	
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low					
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High					
t_{RDE}	Data Bus Enable from READ Control	10		10		
t_1	TIMER-IN Low Time	80	–	40	–	
t_2	TIMER-IN High Time	120		70		

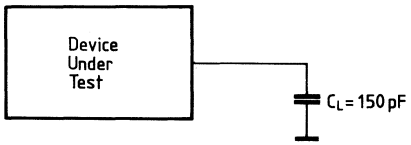
A.C. Testing

Input/Output Waveform



A.C. Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0".
Timing Measurements are made at 2.0 V for Both a Logic "1" and 0.8 V for a Logic "0".

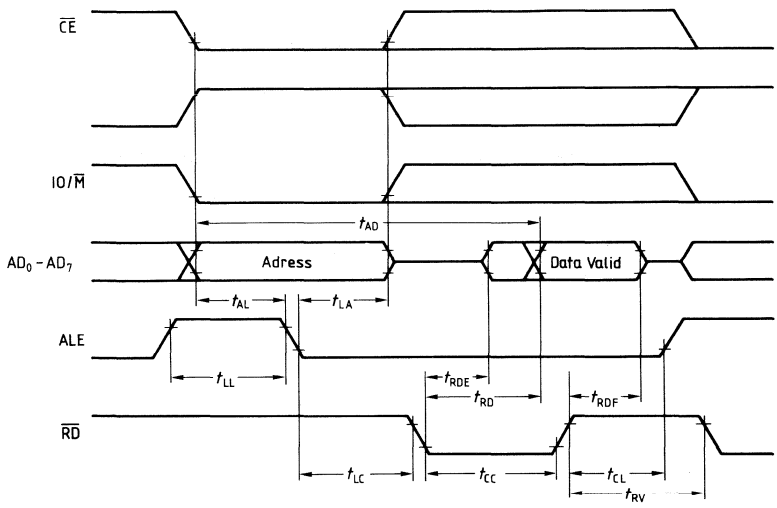
Load Circuit



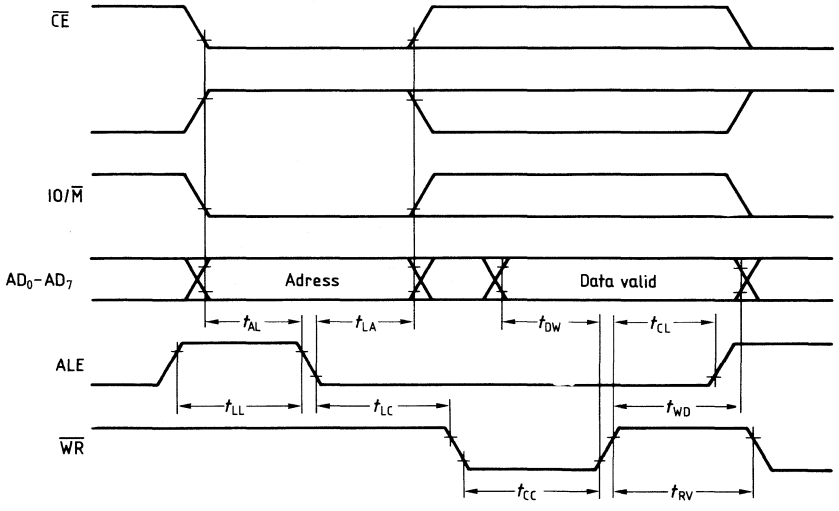
C_L = 150 pF
C_L = Includes JIG Capacitance

Waveforms

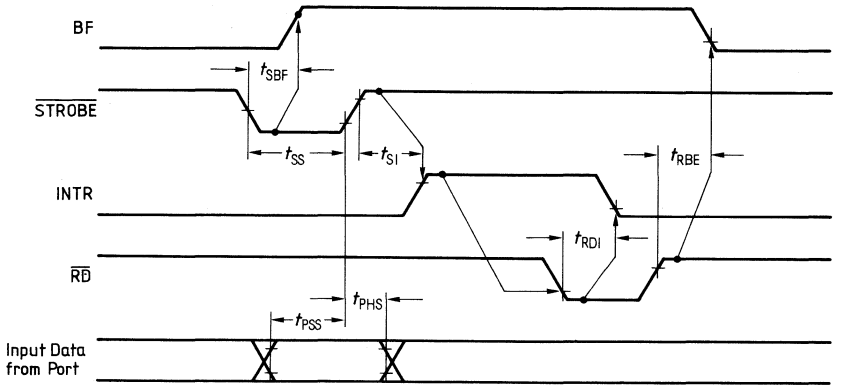
Read Cycle



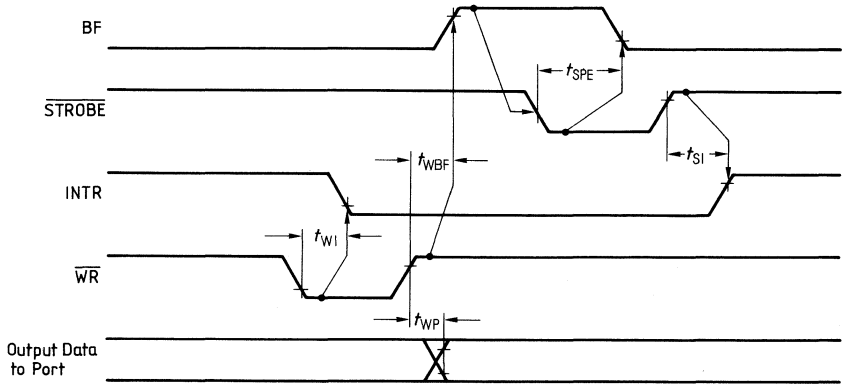
Write Cycle



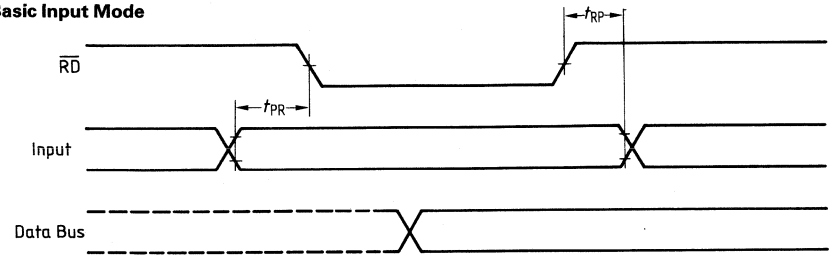
Strobed Input Mode



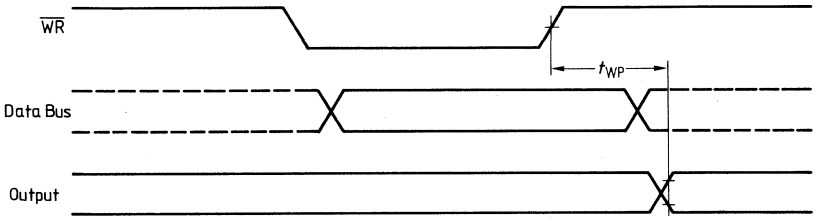
Strobed Output Mode



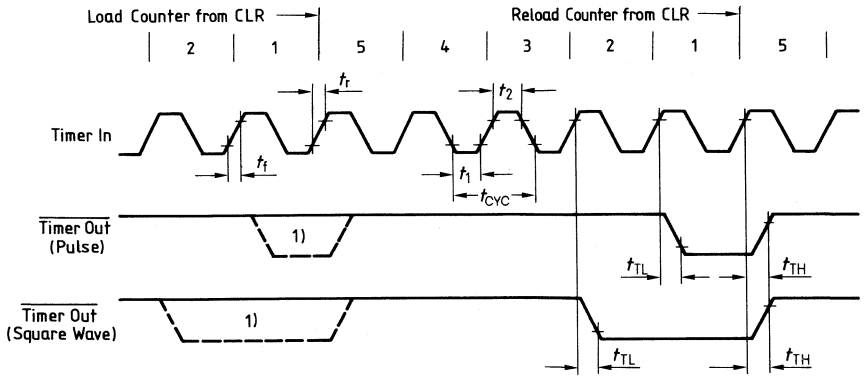
Basic Input Mode



Basic Output Mode



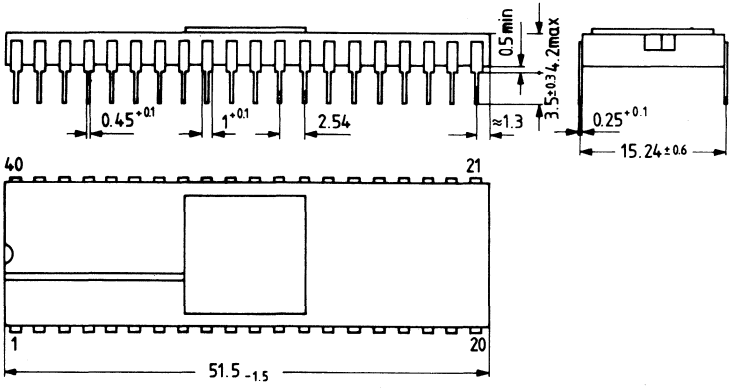
Timer Output Countdown from 5 to 1



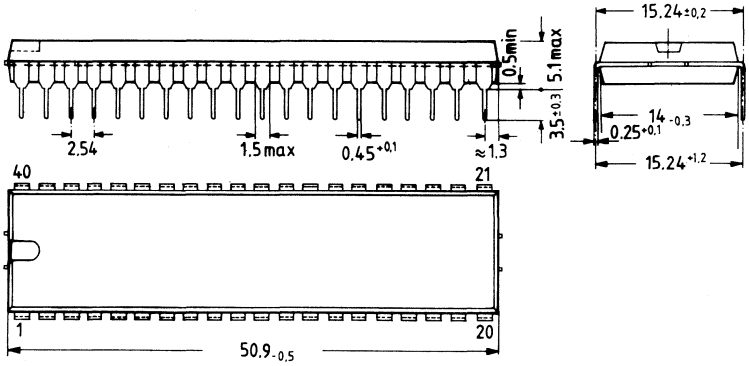
1) The Timer Output is periodic if an automatic reload Mode (M1 Mode Bit = 1)

Package Outline

40 Pin Ceramic Package Type C



40 Pin Plastic Package Type P



Ordering Description

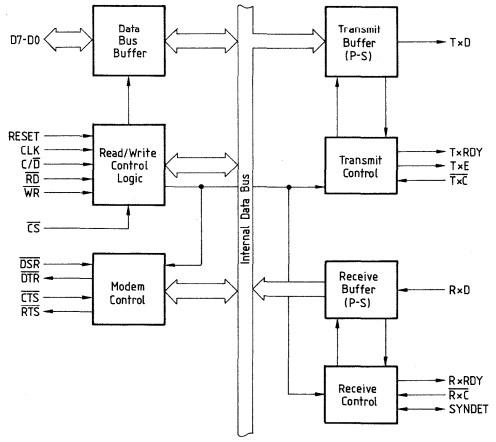
Type	Description	Ordering Number
	RAM with I/O Port and Timer	
SAB 8155-C	Ceramic	Q 67120-Q 43
SAB 8155-P	Plastic	Q 67120-Q 42
SAB 8155-2-C	Ceramic	Q 67120-Q 85
SAB 8155-2-P	Plastic	Q 67120-Q 86

Advance Information

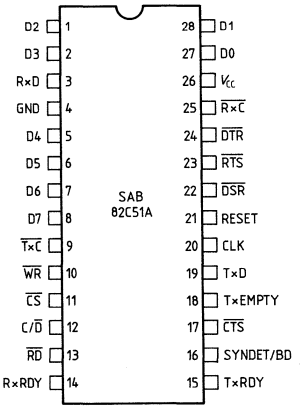
SAB 82C51A Programmable Communications Interface

- Synchronous and asynchronous operation
- Synchronous 5-bit to 8-bit characters; internal or external character synchronization; automatic sync insertion
- Asynchronous 5-bit to 8-bit characters; clock rate 1, 16 or 64 times baud rate; break character generation; 1, 1½ or 2 stop bits; false start bit detection; automatic break detect and handling
- Synchronous baud rate DC to 64 Kbaud
- Asynchronous baud rate DC to 19.2 Kbaud
- Full-duplex, double-buffered transmitter and receiver
- Error detection parity, overrun and framing
- Compatible with an extended range of Siemens microprocessors
- CMOS technology
- 28-pin P-DIP package
- All inputs and outputs are TTL-compatible

Block Diagram



Pin Configuration



The Siemens SAB 82C51A is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Siemens microprocessor families such as SAB 8048/8051/8085 and SAB 8086/8088. The SAB 82C51A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using Siemens high-performance CMOS technology.

10.87

Pin Definitions and Functions

System Bus Interface

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>D0-D7</td><td>1, 2, 5, 6, 7,
8, 27, 28</td><td>I/O</td><td>DATA 0 TO 7
Bidirectional tristate data bus lines.</td></tr>
<tr><td>$\overline{WR}$</td><td>10</td><td>I</td><td>$\overline{WRITE}$
A low on this input informs the SAB 82C51A that the CPU is writing data or control words to the SAB 82C51A.</td></tr>
<tr><td>$\overline{CS}$</td><td>11</td><td>I</td><td>$\overline{CHIP\ SELECT}$
A low on this input selects the SAB 82C51A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the data bus is in the float state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.</td></tr>
<tr><td>C/$\overline{D}$</td><td>12</td><td>I</td><td>CONTROL/$\overline{DATA}$
This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the SAB 82C51A that the word on the data bus is either a data character, control word or status information.
1 = Control/Status; 0 = Data.
<table>
<tr><th>C/$\overline{D}$</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th></th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>SAB 82C51A Data → Data Bus</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus → SAB 82C51A Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Status → Data Bus</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus → Control</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>0</td><td>Data Bus → Tristate</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>1</td><td>Data Bus → Tristate</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$</td><td>13</td><td>I</td><td>$\overline{READ}$
A low on this input informs the SAB 82C51A that the CPU is reading data or status information from the SAB 82C51A.</td></tr>
<tr><td>CLK</td><td>20</td><td>I</td><td>CLOCK
The CLK input is used to generate internal device timing and is normally connected to the phase 2 (TTL) output of the clock generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the receiver or transmitter data bit rates.</td></tr>
<tr><td>RESET</td><td>21</td><td>I</td><td>RESET
An high on this input forces the SAB 82C51A into an idle mode. The device will remain idle until a new set of control words is written into the SAB 82C51A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).
A command reset operation also puts the device into the idle state.</td></tr>
</table>

Modem Control

Symbol	Pin	Input (I) Output (O)	Function
$\overline{CTS}$	17	I	$\overline{CLEAR\ TO\ SEND}$ A low on this input enables the SAB 82C51A to transmit serial data if the TxEnable bit in the command byte is set to a "one". If either a TxEnable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to TxDisable command before shutting down.
$\overline{DSR}$	22	I	$\overline{DATA\ SET\ READY}$ The $\overline{DSR}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a status read operation. The $\overline{DSR}$ input in normally used to test modern conditions such as data set ready.
$\overline{RTS}$	23	O	$\overline{REQUEST\ TO\ SEND}$ The $\overline{RTS}$ output signal is a general-purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the command instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as request to send.
$\overline{DTR}$	24	O	$\overline{DATA\ TERMINAL\ READY}$ The $\overline{DTR}$ output signal is a general-purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the command instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as data terminal ready.

Transmit Control

Symbol	Pin	Input (I) Output (O)	Function
$\overline{TxC}$	9	I	$\overline{TRANSMITTER\ CLOCK}$ The transmitter clock controls the rate at which the character is to be transmitted. In the synchronous transmission mode, the baud rate (1x) is equal to the $\overline{TxC}$ frequency. In asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$. For example: If the baud rate equals 110 baud, $\overline{TxC}$ equals 110 Hz in the 1x mode, $\overline{TxC}$ equals 1.72 kHz in the 16x mode, $\overline{TxC}$ equals 7.04 kHz in the 64x mode. The falling edge of $\overline{TxC}$ shifts the serial data out of the SAB 82C51A.
TxRDY	15	O	TRANSMITTER READY This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by TxEnable; or, for polled operation, the CPU can check TxRDY using a status read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU. Note that when using the polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the empty/full status of the Tx data input register.
TxEMPTY	18	O	TRANSMITTER EMPTY When the SAB 82C51A has no characters to send, the TxEMPTY output will go high. It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplex operational mode. In the synchronous mode, a high on this output indicates that a character has not been loaded and the sync character or characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go low when the sync characters are being shifted out.
TxD	19	O	TRANSMIT DATA This pin is used to transmit the serial data. Serial output data on TxD is changed from parallel data to serial data. In accordance with this, the TxD line will be held in the marking state ('1' level) upon one of the following events: – master reset – CTS signal is high ($\overline{CTS}$ = 1) – TxDisable (TxEN = 0) – TxEMPTY signal is high (TxEMPTY = 1)

Receive Control

Symbol	Pin	Input (I) Output (O)	Function
RxD	3	I	RECEIVE DATA This pin is used to receive the serial data. Serial input data on this line is changed to parallel data according to the format specified by the control words, and then transferred to the receive data buffer.
RxRDY	14	O	RECEIVER READY This output indicates that the SAB 82C51A contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a status read operation. RxEnable, when off, holds RxRDY in the reset condition. For asynchronous mode, to set RxRDY, the receiver must be enabled to sense a start bit and a complete character must be assembled and transferred to the data output register. For synchronous mode, to set RxRDY, the receiver must be enabled and a character must finish assembly and be transferred to the data output register. Failure to read the character received from the Rx data output register prior to the assembly of the next Rx data character will set overrun condition error and the previous character will be written over and lost. If the Rx data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.
SYNDET/BD	16	I/O	SYNC DETECT/BREAK DETECT This pin is used for SYNDET in synchronous mode and may be used as either input or output, programmable through the control word. It is reset to output mode low upon RESET. When used as an output (internal sync mode), the SYNDET pin will go high to indicate that the SAB 82C51A has located the sync character in the receive mode. If the SAB 82C51A is programmed to use double sync characters then SYDET will go high in the middle of the last bit of the second sync character. SYNDET is automatically reset upon a status read operation. When used as an input (external sync mode), a positive going signal will cause the SAB 82C51A to start assembling data characters on the rising edge of the next $\overline{RxC}$. In asynchronous mode this pin is used for BD. This output will go high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break detect may also be read as a status bit. It is reset only upon a master chip reset or RxD returning to a "one" state.

Receive Control (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{RxC}$	25	I	$\overline{RECEIVER\ CLOCK}$ The receiver clock controls the rate at which the character is to be received. In synchronous mode, the baud rate (1x) is equal to the actual frequency of $\overline{RxC}$. In asynchronous mode, the baud rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 the $\overline{RxC}$. For example: The baud rate equals 2400 baud, if $\overline{RxC}$ equals 2400 Hz in the 1x mode, $\overline{RxC}$ equals 38.4 kHz in the 16x mode, $\overline{RxC}$ equals 153.6 kHz in the 64x mode. Data is sampled into the SAB 82C51A on the rising edge of $\overline{RxC}$.

Power Supply

Symbol	Pin	Function
GND	4	GROUND (0 V)
V_{CC}	26	POWER SUPPLY (+5 V)

Operational Description

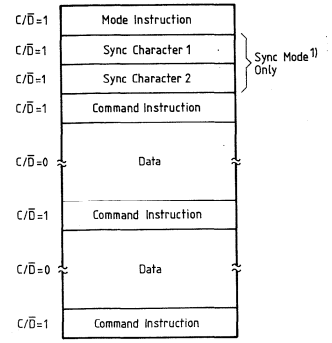
General

The complete functional definition of the SAB 82C51A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the SAB 82C51A to support the desired communications format. These control words will program the baud rate, character length, number of stop bits, synchronous or asynchronous operation, even/odd/off parity, etc. In the synchronous mode, options are also provided to select either internal or external character synchronization.

Once programmed, the SAB 82C51A is ready to perform its communication functions. The TxRDY output is raised high to signal the CPU that the SAB 82C51A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the SAB 82C51A. On the other hand, the SAB 82C51A receives serial data from the modem or I/O device. Upon receiving an entire character, the RxRDY output is raised high to signal the CPU that the SAB 82C51A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The SAB 82C51A cannot begin transmission until the TxEnable (transmitter enable) bit is set in the command instruction and it has received a clear-to-send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon reset.

Typical Data Block



1) The second sync character is skipped if mode instruction has programmed the SAB 82C51A to single character sync mode. Both sync characters are skipped if mode instruction has programmed the SAB 82C51A to async mode.

Programming the SAB 82C51A

Prior to starting data transmission or reception, the SAB 82C51A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the SAB 82C51A and must immediately follow a reset operation (internal or external).

The control words are split into two formats:

1. Mode instruction
2. Command instruction

Mode Instruction

This instruction defines the general operational characteristics of the SAB 82C51A. It must follow a reset operation (internal or external). Once the mode instruction has been written into the SAB 82C51A by the CPU, sync characters or command instructions may be written.

Command Instruction

This instruction defines a word that is used to control the actual operation of the SAB 82C51A.

Both the mode and command instructions must conform to a specified sequence for proper device operation (see figure Typical Data Block). The mode instruction must be written immediately following a reset operation, prior to using the SAB 82C51A for data communication.

All control words written into the SAB 82C51A after the mode instruction will load the command instruction. Command instructions can be written into the SAB 82C51A at any time in the data block during the operation of the SAB 82C51A. To return to the mode instruction format, the master reset bit in the command instruction word can be set to initiate an internal reset operation which automatically places the SAB 82C51A back into the mode instruction format. Command instructions must follow the mode instruction or sync characters.

Mode Instruction Definition

The SAB 82C51A can be used for either asynchronous or synchronous data communication. To understand how the mode instruction defines the functional operation of the SAB 82C51A, the designer can best view the device as two separate components, one asynchronous and the other synchronous, sharing the same package. The format definition can be changed only after a master chip reset. For explanation purposes the two formats will be isolated.

Note:
When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx data line cannot be read on the data bus. In the case of a programmed character length of less than 8 bits, the least significant data bus bits will hold the data; unused bits are "don't care" when writing data to the SAB 82C51A, and will be "zeros" when reading the data from the SAB 82C51A.

Asynchronous Mode (transmit)

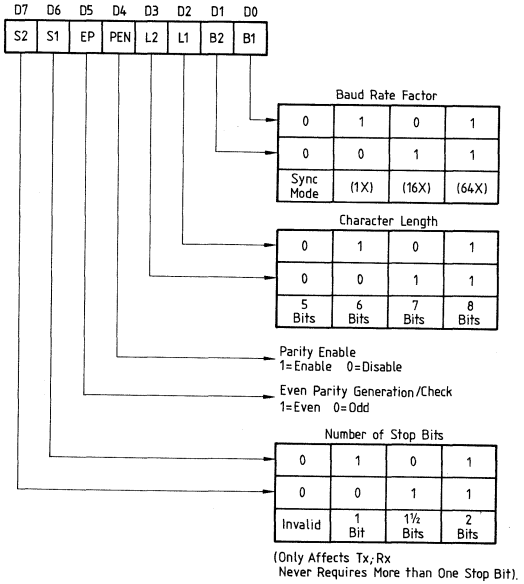
Whenever a data character is sent by the CPU the SAB 82C51A automatically adds a start bit (low level) followed by the data bits (least significant bit first), and the programmed number of stop bits to each character. Also, an even or odd parity bit is inserted prior to the stop bit(s), as defined by the mode instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16 or 1/64 that of the $\overline{TxC}$, as defined by the mode instruction. Break characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the SAB 82C51A the TxD output remains "high" (marking) unless a break (continuously low) has been programmed.

Asynchronous Mode (receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a start bit. The validity of this start bit is checked by again strobing this bit at its nominal center (16x or 64x mode only). If a low is detected again, it is a valid start bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of the $\overline{RxC}$. If a low level is detected as the stop bit the framing error flag will be set. The stop bit signals the end of a character. Note that the receiver requires only one stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the SAB 82C51A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the overrun error

Mode Instruction Format, Asynchronous Mode



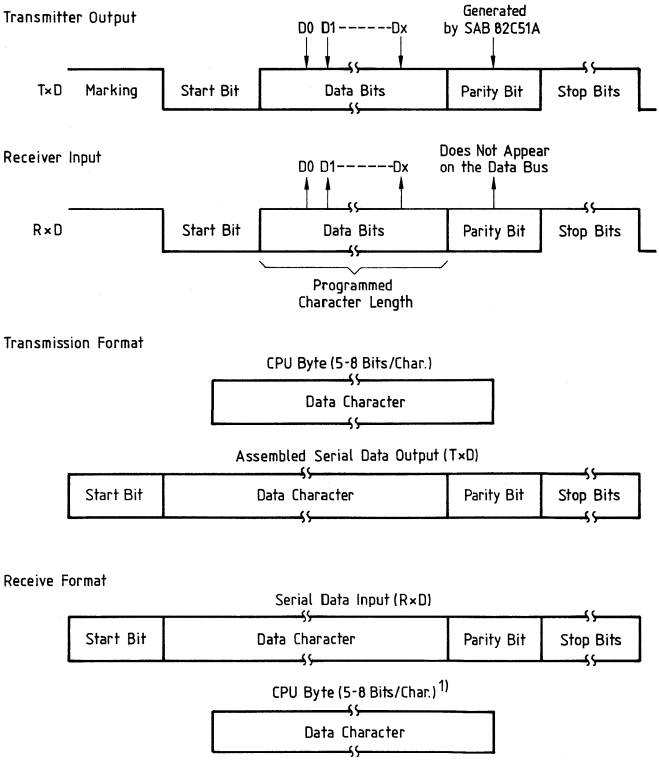
flag is raised (thus the previous character is lost). All of the error flags can be reset by an error reset instruction. The occurrence of any of these errors will not affect the operation of the SAB 82C51A.

Synchronous Mode (transmit)

The TxD output is continuously high until the CPU sends its first character to the SAB 82C51A which usually is a sync character. When the $\overline{CTS}$ line goes low, the first character is transmitted serially. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

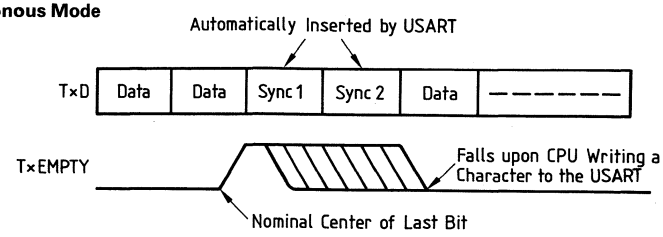
Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the SAB 82C51A with a data character before the SAB 82C51A's transmitter buffers become empty, the sync characters (or character if in single sync character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the SAB 82C51A is empty and sync characters are being sent out. TxEMPTY does not go low when the sync is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the SAB 82C51A.

Asynchronous Mode



1) If character length is defined as 5, 6 or 7 bits the unused bits are set to "zero".

Synchronous Mode

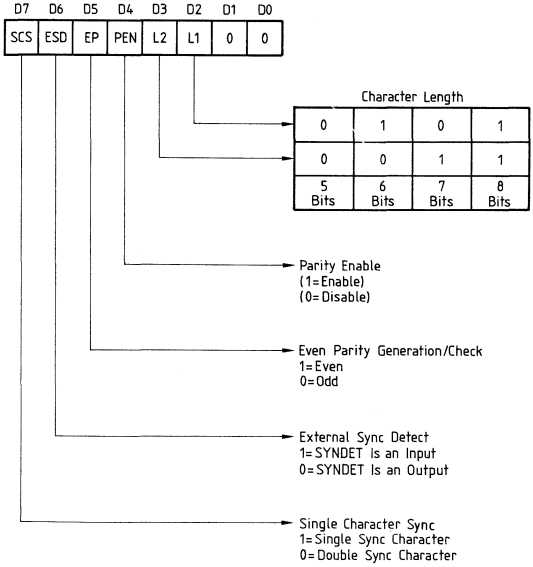


Synchronous Mode (receive)

In this mode, character synchronization can be achieved internally or externally. If the sync mode has been programmed, "enter hunt" command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of $\overline{RxC}$. The contents of the Rx buffer is compared at every bit boundary with the first sync character until a match occurs. If the SAB 82C51A has been programmed for two sync characters, the subsequently received character is also compared; when both sync characters have been detected, the USART ends the hunt mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a "status read". If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external sync mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the SAB 82C51A out of the hunt mode. The high level can be removed after one $\overline{RxC}$ cycle. An "enter hunt" command has no effect in the asynchronous mode of operation.

Mode Instruction Format, Synchronous Mode



Note:
In external sync mode, programming double character sync will affect only the Tx.

Parity error and overrun are both checked in the same way as in the asynchronous Rx mode. Parity is checked when not in hunt, regardless of whether the receiver is enabled or not.

The CPU can command the receiver to enter the hunt mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one", thus preventing a possible false SYNDET caused by data that happens to be in the Rx buffer at "enter hunt" time. Note that the SYNDET flipflop is reset at each status read, regardless of whether internal or external sync has been programmed. This does not cause the SAB 82C51A to return to the hunt mode. When in sync mode, but not in hunt, sync detection is still functional, but only occurs at the "known" word boundaries. Thus, if one status read indicates SYNDET and a second status read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous status read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication). When external SYNDET mode is selected, internal sync detect is disabled, and the SYNDET flipflop may be set at any bit boundary.

Command Instruction Definition

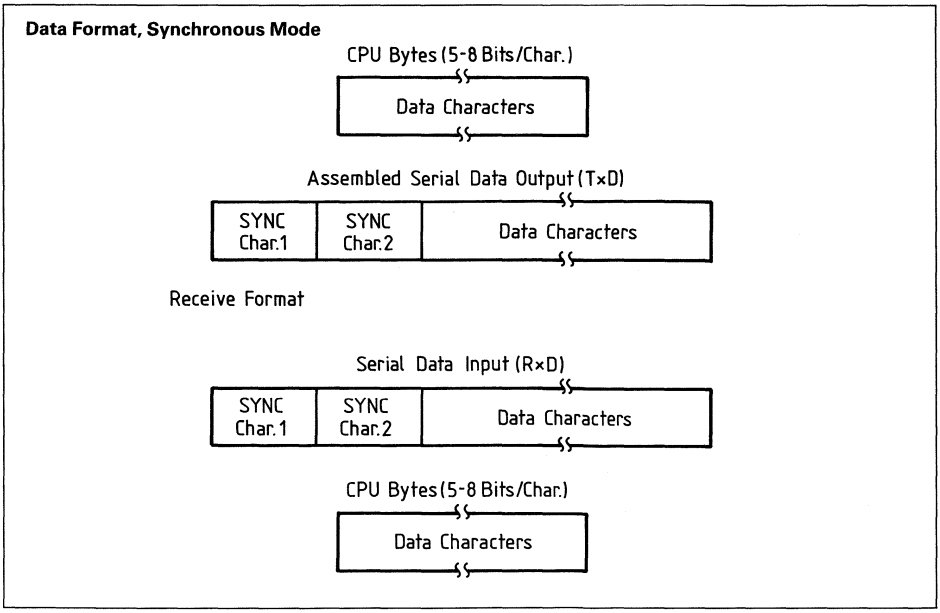
Once the functional definition of the SAB 82C51A has been programmed by the mode instruction and the sync characters are loaded (if in sync mode) then the device is ready to be used for data communication. The command instruction controls the actual operation of the selected format. Functions such as: enable transmit/receive, error reset and modem controls are provided by the command instruction.

Once the mode instruction has been written into the SAB 82C51A and sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D} = 1$) will load a command instruction. A reset operation (internal or external) will return the SAB 82C51A to the mode instruction format.

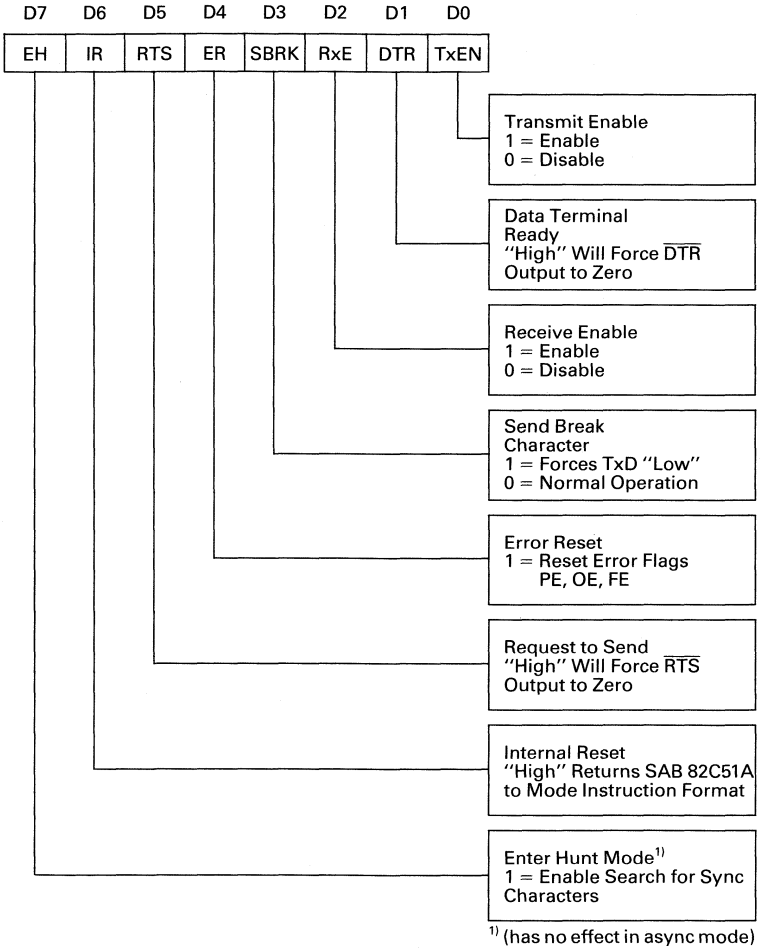
Note:
Internal reset on power-up:

When power is first applied, the SAB 82C51A may come up in the mode, sync character or command format. To guarantee that the device is in the command instruction format before the reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with $C/\overline{D} = 1$ configures sync operation and writes two dummy 00H sync characters. An internal reset command (40H) may then be issued to return the device to the "idle" state.

Data Format, Synchronous Mode



Command Instruction Format



1) (has no effect in async mode)

Note: Error reset must be performed whenever RxEnable and "enter hunt" are programmed.

Status Read Definition

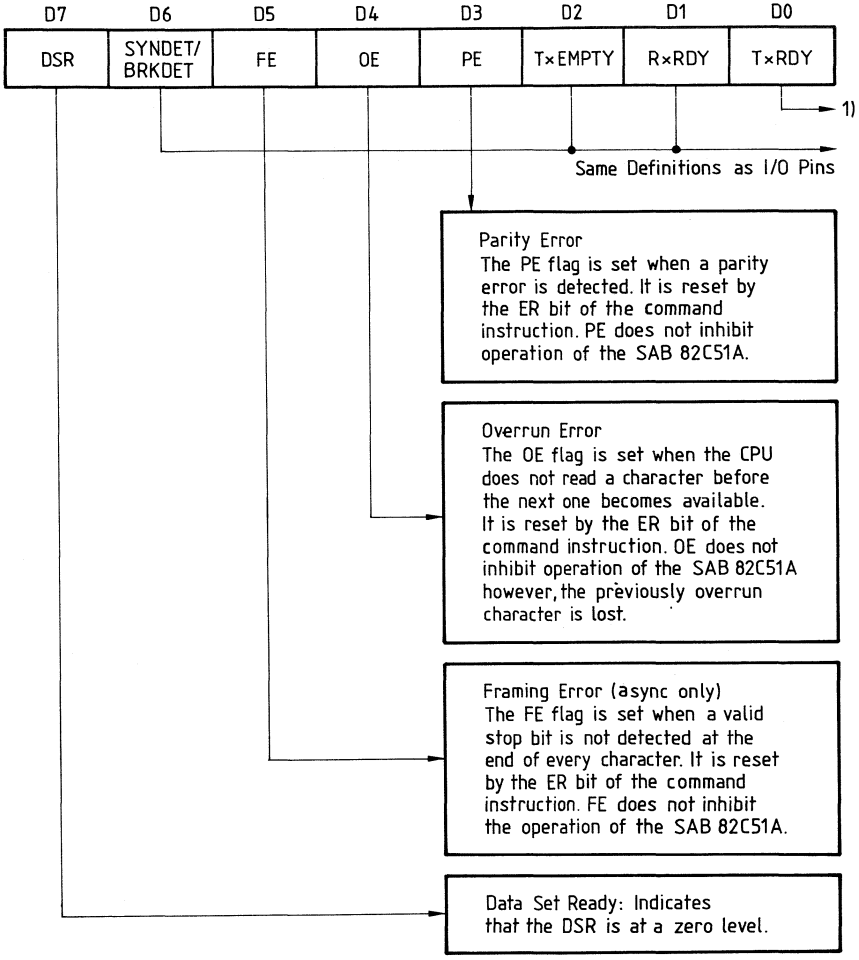
In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The SAB 82C51A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (Status update is inhibited during status read).

A normal "read" command is issued by the CPU with C/$\overline{D}$ = 1 to accomplish this function.

Some of the bits in the status read format have identical meanings to external output pins so that the SAB 82C51A can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.

Status Read Format



Note:
TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both $\overline{CTS}$ and TxEN.
i.e. TxRDY status bit = DB buffer empty
TxRDY pin out = DB buffer empty · ($\overline{CTS}$ = 0) · (TxEN = 1)

Absolute Maximum Ratings

Ambient temperature under bias	0°C to +70°C
Storage temperature	−65°C to +150°C
Supply voltage	−0.5 to +8.0 V
Operating voltage	4 V to 7 V
Voltage on any input	V_{SS} − 2 V to V_{CC} + 0.5 V
Voltage on any output	V_{SS} − 0.5 V to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 V + 10%; V_{SS} = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} + 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{OFL}	Output float leakage	–	±10	µA	V_{OUT} = V_{CC} to 0 V
I_{IL}	Input leakage	–	±1	µA	V_{IN} = V_{CC} to 0 V
I_{CCO}	Operating supply current	–	5	mA	Asynchronous x64 during transmitting/ receiving; outputs open
I_{CCS}	Standby supply current	–	100	µA	Input voltage at V_{CC} or GND level; outputs open

Capacitance

T_A = 25°C, V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_C = 1 MHz
C_{IO}	I/O capacitance	–	20	pF	Unmeasured pins returned to GND

AC Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0V ±10%, GND = 0V

Bus Parameters [1]

Read Cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AR}	Address stable before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0	–	ns	[2]
t_{RA}	Address hold time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0	–	ns	[2]
t_{RR}	$\overline{READ}$ pulse width	150	–	ns	–
t_{RD}	Data delay from $\overline{READ}$	–	140	ns	[3] C_L = 150 pF
t_{DF}	$\overline{READ}$ to data floating	10	50	ns	–

Write Cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AW}	Address stable before $\overline{WRITE}$	0	–	ns	–
t_{WA}	Address hold time for $\overline{WRITE}$	0	–	ns	–
t_{WW}	$\overline{WRITE}$ pulse width	150	–	ns	–
t_{DW}	Data setup time for $\overline{WRITE}$	80	–	ns	–
t_{WD}	Data hold time for $\overline{WRITE}$	10	–	ns	–
t_{RV}	Recovery time between writes	6	–	t_{CY}	[4]
t_{RESW}	Reset pulse width	6	–	t_{CY}	[6]

Notes:

[1] AC timings are measured at V_{OH} = 2.0V and V_{OL} = 0.8V with 150 pF capacitance load.

[2] Chip select ($\overline{CS}$) and command/data (C/$\overline{D}$) are considered as addresses.

[3] Assumes that address is valid before $\overline{RD}\downarrow$.

[4] This recovery time is for mode initialization only. Write data is allowed only when TxRDY = 1. Recovery time between writes for asynchronous mode is 8 t_{CY} and for synchronous mode is 16 t_{CY}.

[5] The TxC and RxC frequencies have the following limitations with respect to CLK: For 1x baud rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$.
For 16x and 64x baud rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$.

[6] System clock must be running during reset.

[7] Status update can have a maximum delay of 28 clock periods from the event affecting the status.

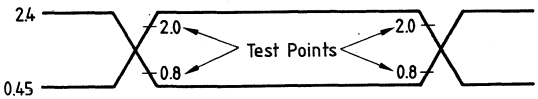
Other Timings

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{CY}	Clock period	125	–	ns	5) 6)
t_{CH}	Clock high pulse width	50	–	ns	–
t_{CL}	Clock low pulse width	35	–	ns	–
t_R, t_F	Clock rise and fall time	–	20	ns	–
t_{DTx}	TxD delay from falling edge of $\overline{TxC}$	–	0.5	µs	–
t_{Tx}	Transmitter input clock frequency 1x baud rate 16x baud rate 64x baud rate	 DC DC DC	 240 1536 1536	 kHz kHz kHz	–
t_{TPW}	Transmitter input clock pulse width 1x baud rate 16x and 64x baud rate	 12 1	 – –	 t_{CY} t_{CY}	 – –
t_{TPD}	Transmitter input clock pulse delay 1x baud rate 16x and 64x baud rate	 15 3	 – –	 t_{CY} t_{CY}	 – –
t_{Rx}	Receiver input clock frequency 1x baud rate 16x baud rate 64x baud rate	 DC DC DC	 240 1536 1536	 kHz kHz kHz	 – – –
t_{RPW}	Receiver input clock pulse width 1x baud rate 16x and 64x baud rate	 12 1	 – –	 t_{CY} t_{CY}	 – –
t_{RPD}	Receiver input clock pulse delay 1x baud rate 16x and 64x baud rate	 15 3	 – –	 t_{CY} t_{CY}	 – –
t_{TxRDY}	TxRDY pin delay from center of last bit	–	8	t_{CY}	7)
$t_{xRDY\ CLEAR}$	TxRDY ↓ from leading edge of $\overline{WR}$	–	400	ns	7)
t_{RxRDY}	RxRDY pin delay from center of last bit	–	26	t_{CY}	7)
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from leading edge of $\overline{RD}$	–	200	ns	7)
t_{IS}	Internal SYNDET delay from rising edge of $\overline{RxC}$	–	26	t_{CY}	7)
t_{ES}	External SYNDET setup time after rising edge of $\overline{RxC}$	16	–	t_{CY}	7)
$t_{TxEMPTY}$	TxEMPTY delay from center of last bit	–	20	t_{CY}	7)
t_{WC}	Control delay from rising edge of write (TxEn, $\overline{DTR}$, $\overline{RTS}$)	–	8	t_{CY}	7)
t_{CR}	Control to read setup time ($\overline{DSR}$, $\overline{CTS}$)	20	–	t_{CY}	7)
t_{RxDS}	RxD setup time for rising edge of $\overline{RxC}$ (1x baud)	11	–	t_{CY}	–
t_{RxDH}	RxD hold time for falling edge of $\overline{RxC}$ (1x baud)	17	–	t_{CY}	–

For notes refer to page 139.

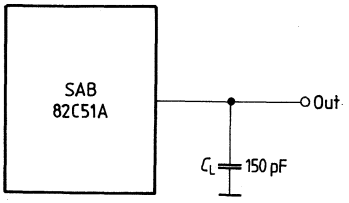
AC Testing

Input/Output Waveform



AC testing: Inputs are driven at 2.4V for a logic "1" and at 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and at 0.8V for a logic "0".

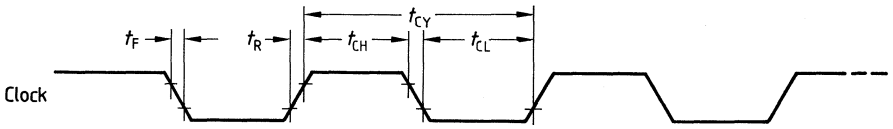
Load Circuit



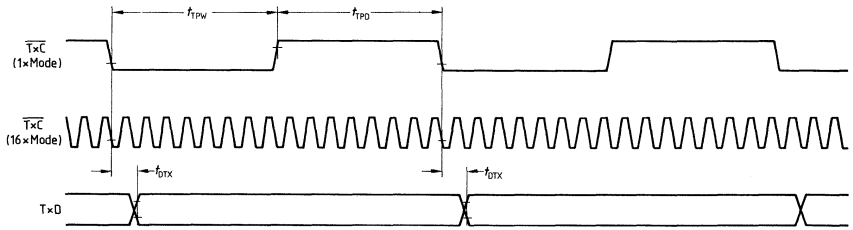
C_L = 150 pF

Waveforms

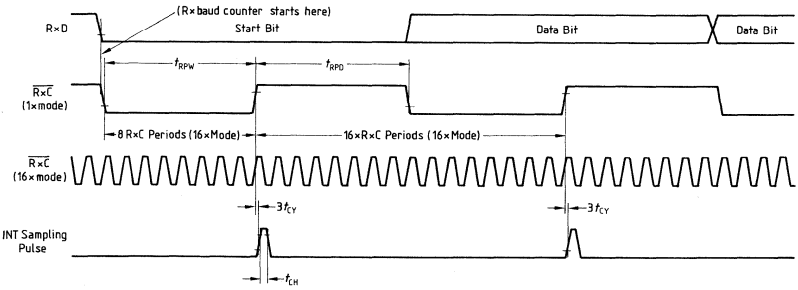
System Clock Input



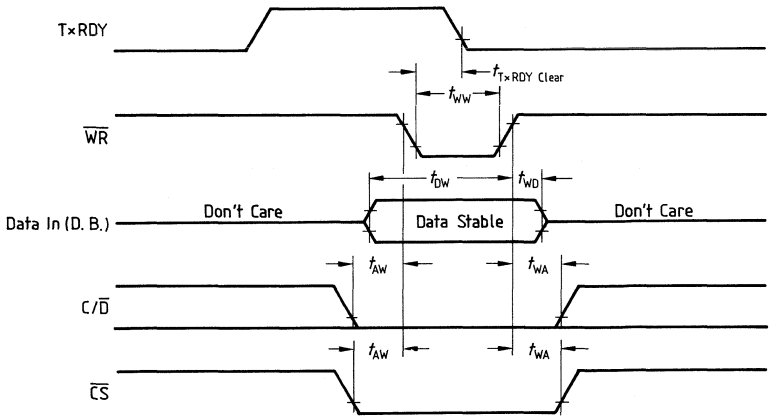
Transmitter Clock and Data



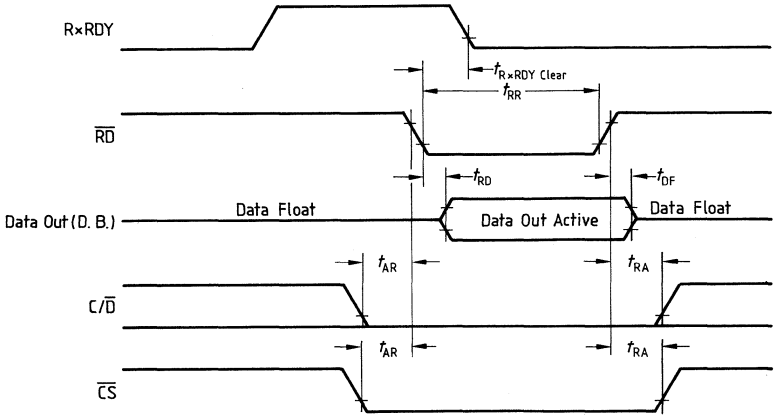
Receiver Clock and Data



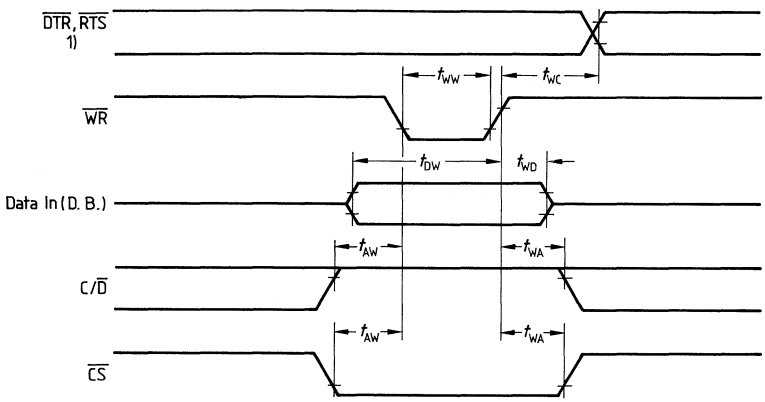
Write Data Cycle (CPU → USART)



Read Data Cycle (CPU ← USART)

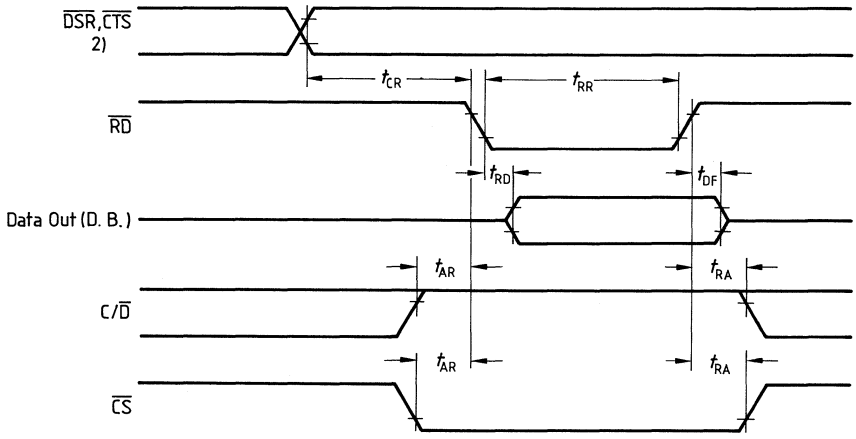


Write Control or Output Port Cycle (CPU → USART)



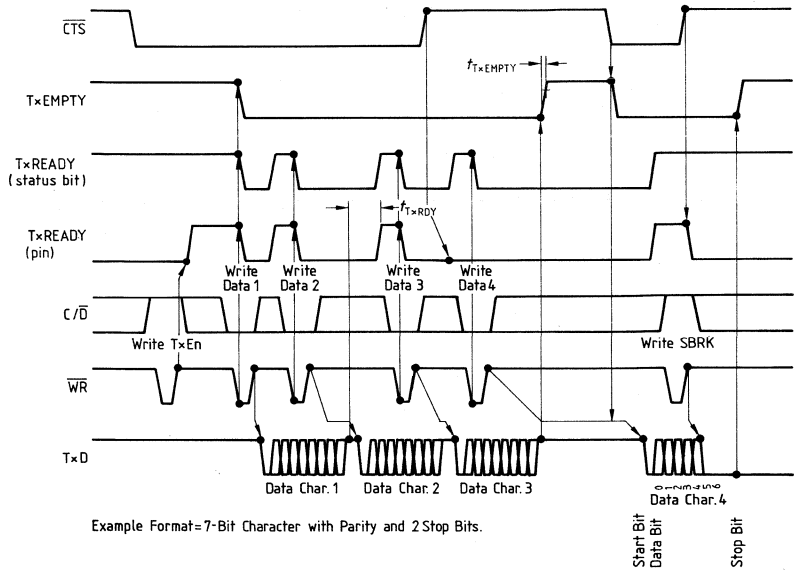
1) t_{WC} Includes the Response Timing of a Control Byte.

Read Control or Input Port (CPU ← USART)



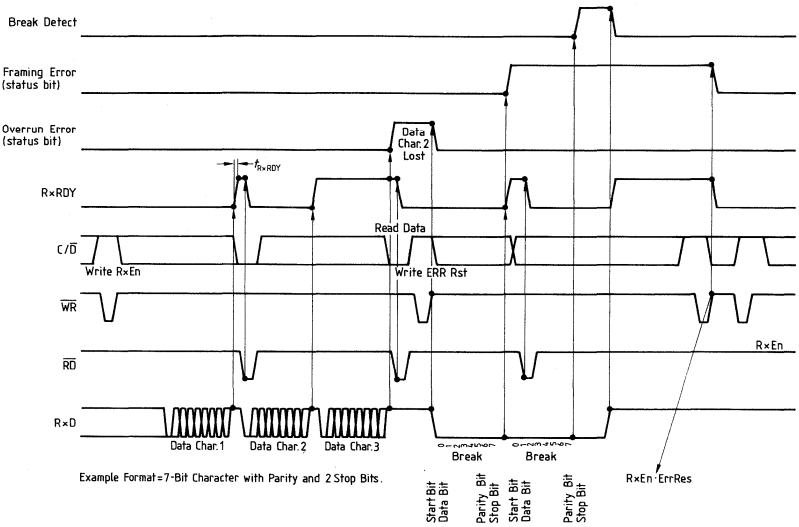
2) t_{CR} Includes the Effect of CTS on the T×ENBL Circuitry.

Transmitter Control and Flag Timing (async mode)

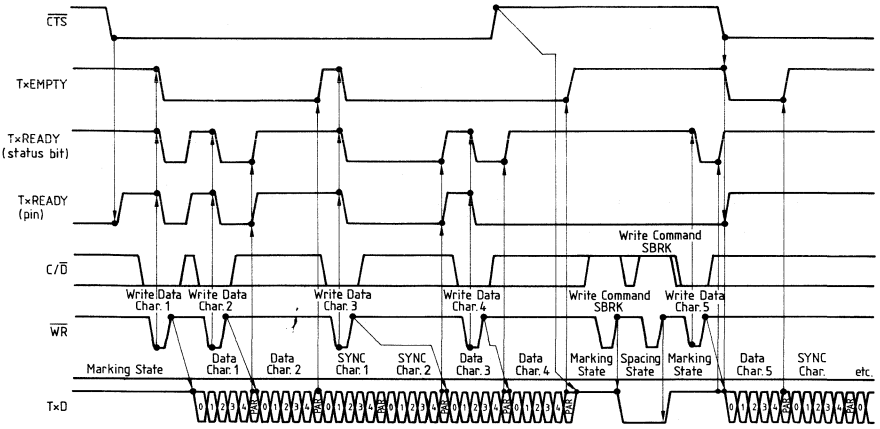


Example Format = 7-Bit Character with Parity and 2 Stop Bits.

Receiver Control and Flag Timing (async mode)

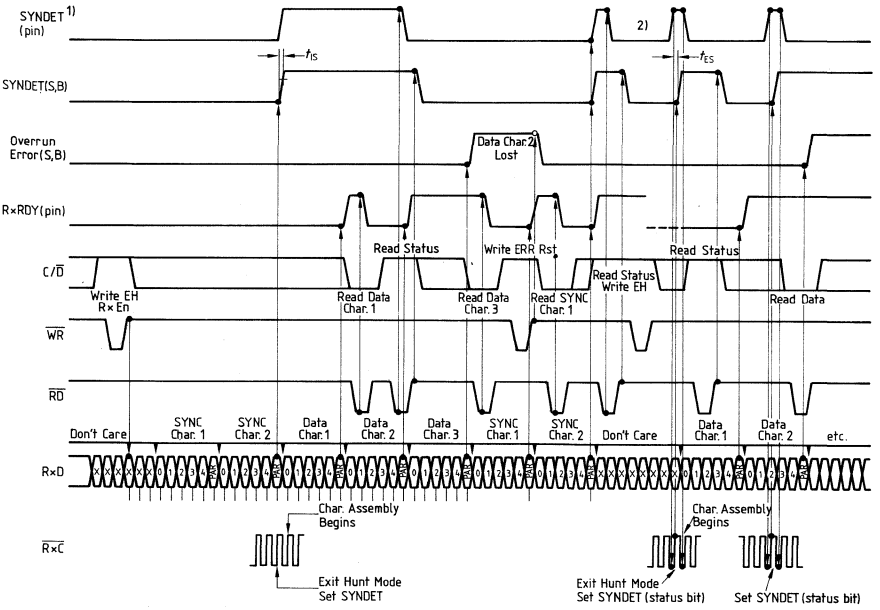


Transmitter Control and Flag Timing (sync mode)



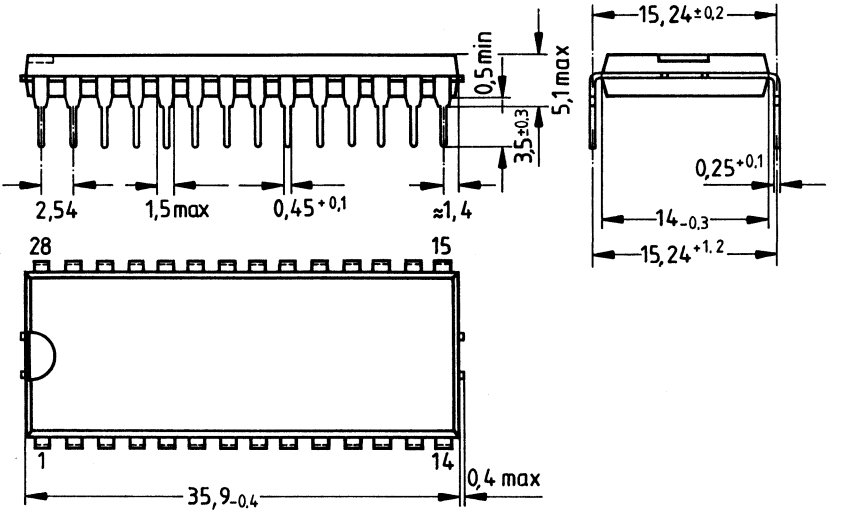
Example Format = 5 Bit Character with Parity, 2 Sync Characters.

Receiver Control and Flag Timing (sync mode)



Package Outlines

Plastic Package, P-DIP-28
(dual-in-line package)
20 B 28 DIN 41870 T 10



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 82C51A-P	Q67120-P216	Programmable communications interface

Preliminary

SAB 82C53 Programmable CMOS Interval Timer

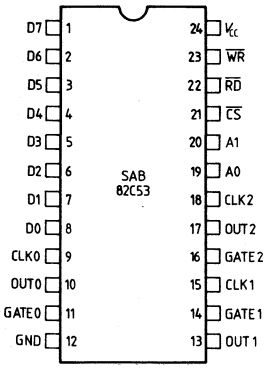
SAB 82C53: Command Width 400 ns

- Compatible with all Siemens and most other microprocessors
- Three independent 16-bit counters
- Handles inputs from DC to 2.6 MHz

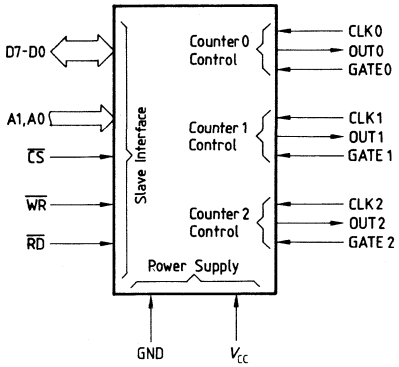
SAB 82C53-5: Command Width 300 ns

- Low power CMOS (I_{CC} = 10 mA at max. count frequency)
- Completely TTL compatible
- Six programmable counter modes
- Binary or BCD counting

Pin Configuration



Logic Symbol



The SAB 82C53 is a high-performance, CMOS version of the industry standard 8253 timer/counter which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 2.6 MHz. All modes are software-programmable. The SAB 82C53 is pin-compatible with the NMOS 8253, and is a subset of the SAB 82C54.

Six programmable timer modes allow the SAB 82C53 to be used as an event counter, elapsed time indicator, programmable monoflop, and in many other applications.

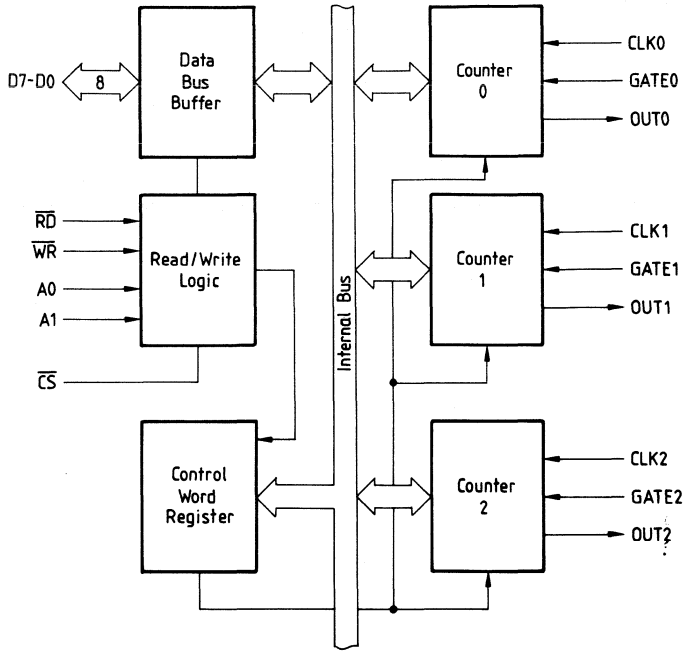
The SAB 82C53 is fabricated in Siemens advanced CMOS technology which provides low power consumption and is packaged in a 24-pin dual-in-line plastic package.

12.87

Pin Definitions and Functions

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>D7-D0</td><td>1-8</td><td>I/O</td><td>DATA 7-0
Bidirectional tristate data bus lines, connected to system data bus.</td></tr>
<tr><td>CLK 0</td><td>9</td><td>I</td><td>CLOCK 0
Clock input of counter 0.</td></tr>
<tr><td>OUT 0</td><td>10</td><td>O</td><td>OUTPUT 0
Output of counter 0.</td></tr>
<tr><td>GATE 0</td><td>11</td><td>I</td><td>GATE 0
Gate input of counter 0.</td></tr>
<tr><td>OUT 1</td><td>13</td><td>O</td><td>OUTPUT 1
Output of counter 1.</td></tr>
<tr><td>GATE 1</td><td>14</td><td>I</td><td>GATE 1
Gate input of counter 1.</td></tr>
<tr><td>CLK 1</td><td>15</td><td>I</td><td>CLOCK 1
Clock input of counter 1.</td></tr>
<tr><td>GATE 2</td><td>16</td><td>I</td><td>GATE 2
Gate input of counter 2.</td></tr>
<tr><td>OUT 2</td><td>17</td><td>O</td><td>OUTPUT 2
Output of counter 2.</td></tr>
<tr><td>CLK 2</td><td>18</td><td>I</td><td>CLOCK 2
Clock input of counter 2.</td></tr>
<tr><td>A1, A0</td><td>20-19</td><td>I</td><td>ADDRESS 1, 0
Used to select one of the three counters or the control word register for read or write operations. Normally connected to the system address bus.
<table>
<tr><th>A1</th><th>A0</th><th>Selects</th></tr>
<tr><td>0</td><td>0</td><td>Counter 0</td></tr>
<tr><td>0</td><td>1</td><td>Counter 1</td></tr>
<tr><td>1</td><td>0</td><td>Counter 2</td></tr>
<tr><td>1</td><td>1</td><td>Control Word Register</td></tr>
</table></td></tr>
<tr><td>$\overline{CS}$</td><td>21</td><td>I</td><td>$\overline{CHIP\ SELECT}$
A low on this input enables the SAB 82C53 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.</td></tr>
<tr><td>$\overline{RD}$</td><td>22</td><td>I</td><td>$\overline{READ\ CONTROL}$
This input is low during CPU read operations.</td></tr>
<tr><td>$\overline{WR}$</td><td>23</td><td>I</td><td>$\overline{WRITE\ CONTROL}$
This input is low during CPU write operations.</td></tr>
<tr><td>V_{CC}</td><td>24</td><td>–</td><td>POWER SUPPLY (+5V)</td></tr>
<tr><td>GND</td><td>12</td><td>–</td><td>GROUND (0 V)</td></tr>
</table>

Block Diagram



Functional Description

General

The SAB 82C53 is a programmable interval timer/counter designed for use with Siemens and other microcomputer systems. It is a general-purpose, multitiming element that can be treated as an array of I/O ports in the system software.

The SAB 82C53 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the SAB 82C53 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the SAB 82C53 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other timer/counter functions common to microcomputers which can be implemented with the SAB 82C53 are:

- Real time clock
- Event counter
- Digital monoflop
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Slave Interface

The bidirectional tristate data bus buffer is used to interface the SAB 82C53 to the system bus.

The read/write logic accepts inputs from the system bus and generates control signals for the other functional blocks of the SAB 82C53. A1 and A0 select one of the three counters or the control word register for read or write accesses. An active (low) $\overline{RD}$ input allows the CPU to read one of the counters. An active (low) $\overline{WR}$ input allows the CPU to write into one of the control word registers. $\overline{RD}$ and $\overline{WR}$ are ignored unless the SAB 82C53 is selected by an active (low) $\overline{CS}$ input.

Control Word Register

The control word register is selected by the read/write logic with A1, A0 = 11. A CPU write operation stores a control word into the control word register. These control words specify the operating mode of the counters.

The control word register can only be written to; no read operation of its contents is available.

Counters

These three functional blocks are identical in operation, so only a single counter will be described.

The counters are fully independent. Each counter may operate in a different mode. The internal block diagram of a single counter is shown in the following figure. The control word register shown in the figure is not part of the counter itself, but determines the operating mode of the counter.

The actual counter is labelled CE (for "counting element"). It is a 16-bit presettable synchronous down counter.

Output latch M and output latch L are two 8-bit latches. The designations M and L stand for "most significant byte" and "least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable counter latch command is sent to the SAB 82C53, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's control logic to drive the internal bus. This is how the 16-bit counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called count register M and count register L. Both are normally referred to as one unit and called just CR. When a new count is written to the counter, the count is stored in the CR and later transferred to the CE. The control logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR M and CR L are cleared when the counter is programmed. In this way, if the counter has been programmed for one byte counts (either most significant byte only or least significant byte only), the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

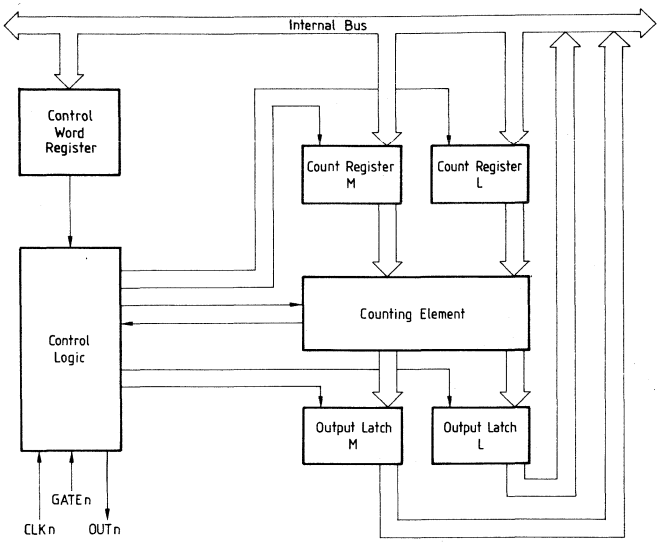
The control logic is also shown in the diagram. CLKn, GATEn, and OUTn are all connected to the outside world through the control logic.

System Interface

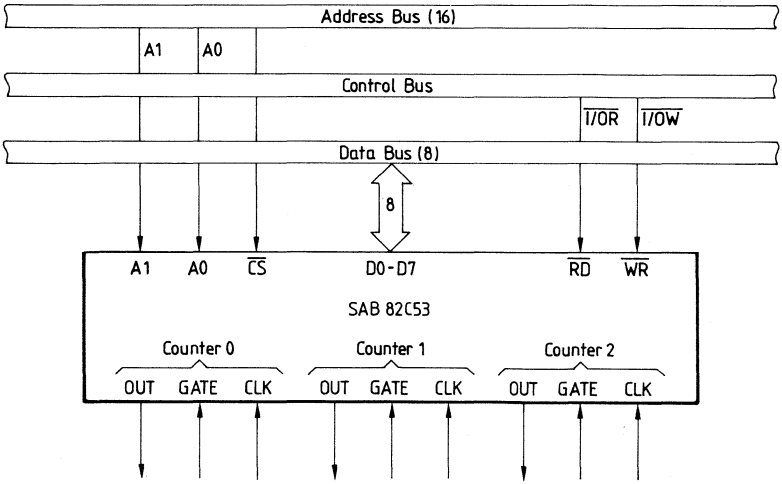
The SAB 82C53 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for mode programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder for larger systems.

Internal Block Diagram of a Counter



SAB 82C53 System Interface



Operational Description

General

After power-up, the state of the SAB 82C53 is undefined. The mode, count value, and output of all counters are undefined.

The operating mode of each counter is determined when it is programmed. Each counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the SAB 82C53

Counters are programmed by writing a control word and then an initial count. The control word format is shown in the following figure.

All control words are written into the control word register, which is selected with A1, A0 = 11. The control word itself specifies which counter is being programmed.

By contrast, initial counts are written into the counters, not the control word register. The A1, A0 inputs are used to select the counter to be written into. The format of the initial count is determined by the control word used.

Control Word Format

A1, A0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RW – Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see read operations)
0	1	Read/Write Least Significant Byte Only.
1	0	Read/Write Most Significant Byte Only.
1	1	Read/Write Least Significant Byte First, Then Most Significant Byte.

M – Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter, 16-Bit
1	Binary-Coded Decimal (BCD) Counter (4 decades)

NOTE: Don't care bits (X) should be 0 to insure compatibility with future products.

Write Operations

The programming procedure for the SAB 82C53 is very flexible. Only two conventions need to be remembered:

1) For each counter the control word must be written before the initial count is written.
2) The initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the control word register and the three counters have separate addresses (selected by the A1, A0 inputs), and each control word specifies the counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a counter at any time without affecting the counter's programmed mode in any way. Counting will be affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

A Few Possible Programming Sequences

	A1	A0
Control Word – Counter 0	1	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0
Control Word – Counter 1	1	1
LSB of Count – Counter 1	0	1
MSB of Count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 2	1	0

	A1	A0
Control Word – Counter 2	1	1
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 2	1	0
LSB of Count – Counter 1	0	1
MSB of Count – Counter 1	0	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0

	A1	A0
Control Word – Counter 0	1	1
Counter Word – Counter 1	1	1
Control Word – Counter 2	1	1
LSB of Count – Counter 2	1	0
LSB of Count – Counter 1	0	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0
MSB of Count – Counter 1	0	1
MSB of Count – Counter 2	1	0

	A1	A0
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of Count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 1	0	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 0	0	0
MSB of Count – Counter 2	1	0

Note:
In all four examples, all counters are programmed to read/write two-byte counts.
These are only four of many possible programming sequences.

Read Operations

It is often desirable to read the value of a counter without disturbing the count in progress. This is easily done in the SAB 82C53.

There are two possible methods for reading the counters: a simple read operation and the counter latch command.

Each is explained below. The first method is to perform a simple read operation. To read the counter which is selected with the A1, A0 inputs, the CLK input of the selected counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.
Note that reading the control word register is illegal and will return unreliable data.

Counter Latch Command

The second method uses the "counter latch command". Like a control word, this command is written to the control word register, which is selected with A1, A0 = 11. Also like a control word, the SC0, SC1 bits select one of the three counters, but two other bits, D5 and D4, distinguish this command from a control word.

The selected counter's output latch (OL) latches the count at the time the counter latch command is received. This count is held in the latch until it is read by the CPU (or until the counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the counters "on the fly" without affecting counting in progress. Multiple counter latch commands may be used to latch more than one counter. Each latched counter's OL holds its count until it is read. Counter latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second counter latch command is ignored. The count read will be the count at the time the first counter latch command was issued.

With either method, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other counters may be inserted between them.

Another feature of the SAB 82C53 is that reads and writes of the same counter may be interleaved; for example, if the counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte
2. Write new least significant byte
3. Read most significant byte
4. Write new most significant byte

If a counter is programmed to read/write two-byte counts, the following precaution applies; a program must not transfer control between reading the first and second byte to another routine which also reads from that same counter. Otherwise, an incorrect count will be read.

Counter Latch Command Format

A1, A0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 = specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Illegal

D5, D4 = 00 designates counter latch command

X = don't care

Note:
Don't care bits (X) should be 0 to insure compatibility with future products.

Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Description
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No Operation (tristate)
1	X	X	X	X	No Operation (tristate)
0	1	1	X	X	No Operation (tristate)

Mode Definitions

The following are defined for use in describing the operation of the SAB 82C53.

CLK pulse: a rising edge, then a falling edge, in that order, of a counter's CLK input.

Trigger: a rising edge of a counter's GATE input.

Counter loading: the transfer of a count from the CR to the CE (refer to the "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the control word is written, OUT is initially low, and will remain low until the counter reaches zero. OUT then goes high and remains high until a new count or a new mode 0 control word is written into the counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the control word and initial count are written to a counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

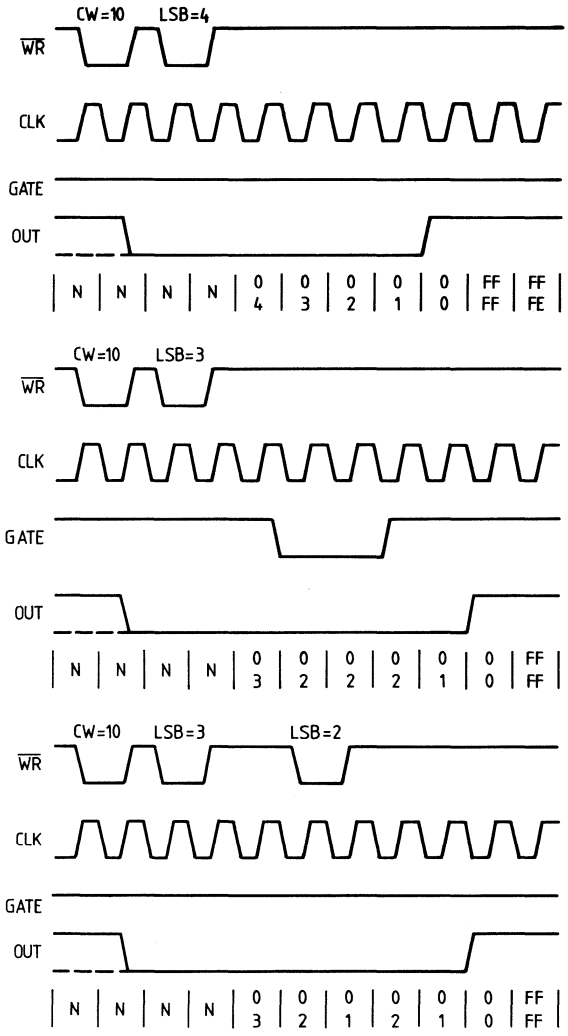
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

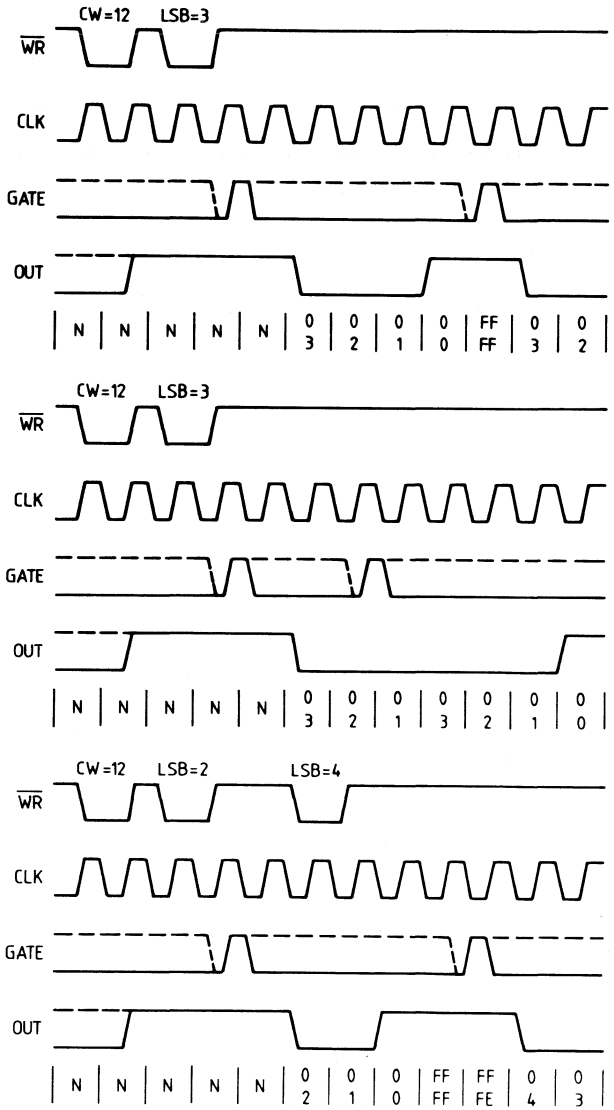
If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

Note:
The following conventions apply to all Mode Timing Diagrams:
1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant bytes (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "control word"; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values.
The lower number is the least significant byte.
The upper number is the most significant byte.
Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Mode 0 Timing Diagram



Mode 1 Timing Diagram



Mode 1: Hardware-Retriggerable Single-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the single-shot pulse, and will remain low until the counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the control word and initial count, the counter is armed. A trigger results in loading the counter and setting OUT low on the next CLK pulse, thus starting the single-shot pulse. An initial count of N will result in a single-shot pulse N CLK cycles in duration. The single-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The single-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the counter during a single-shot pulse, the current single-shot is not affected unless the counter is retriggered. In that case, the counter is loaded with the new count and the pulse continues until the new count expires.

Mode 2: Rate Generator

This mode functions like a divide-by-N counter. It is typically used to generate a real-time clock interrupt. OUT will initially be high. When the initial count has decrement to 1, OUT goes low for one CLK pulse. OUT then goes high again, the counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated infinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the counter.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

Mode 3: Square Wave Mode

Mode 3 is typically used for baud rate generation. Mode 3 is similar to mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated infinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the counter.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This allows the counter to be synchronized by software also.

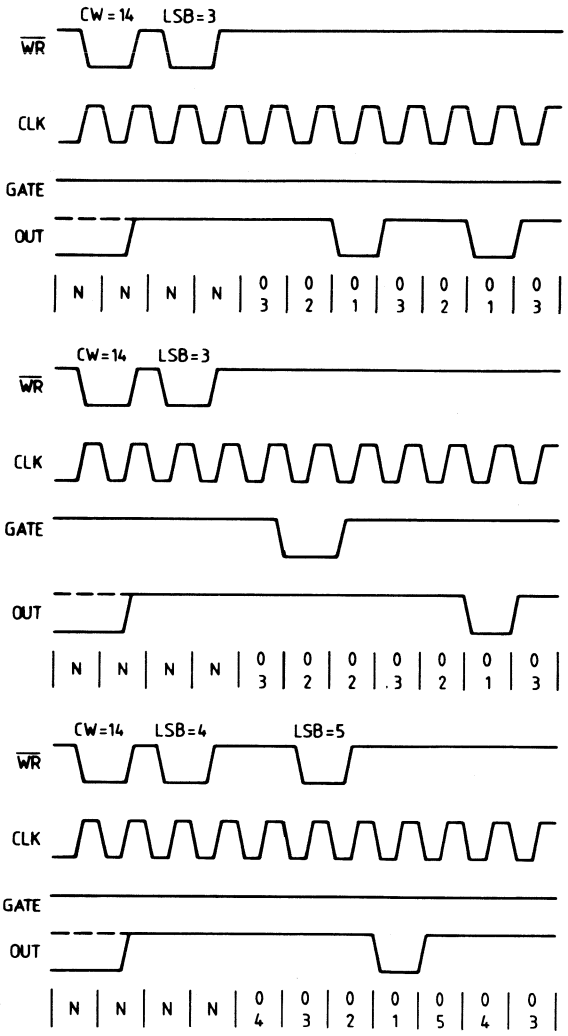
Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the counter is reloaded with the initial count. The above process is repeated infinitely.

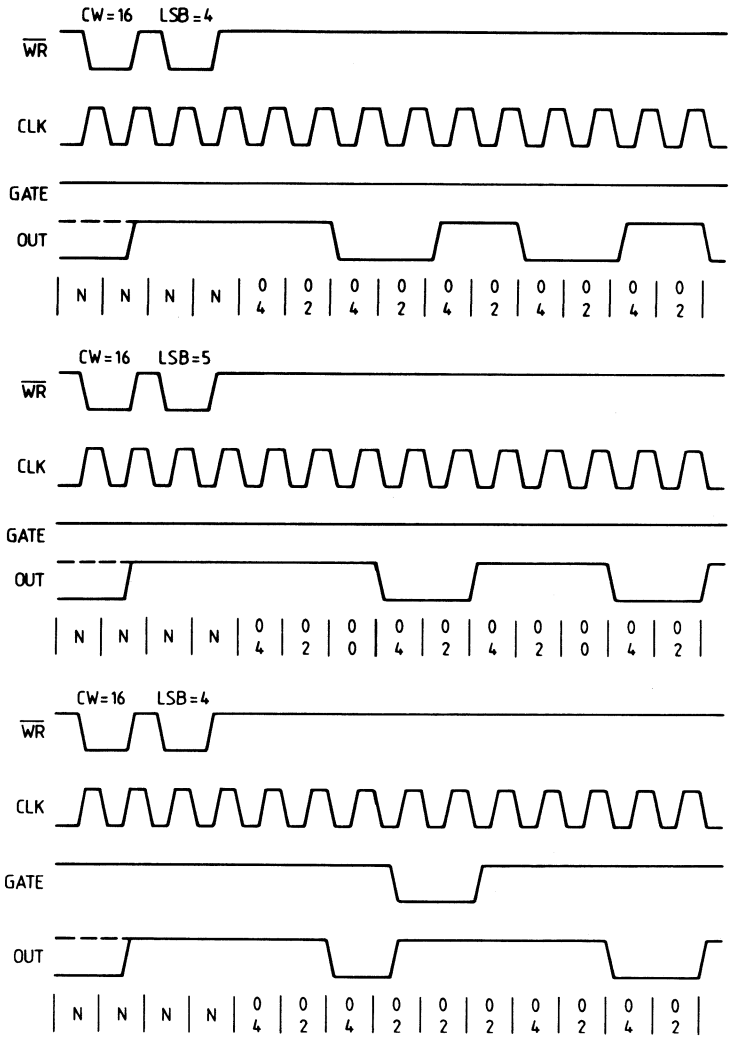
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the counter is reloaded with the initial count minus one. The above process is repeated infinitely. So for odd counts, OUT will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

Mode 2 Timing Diagram



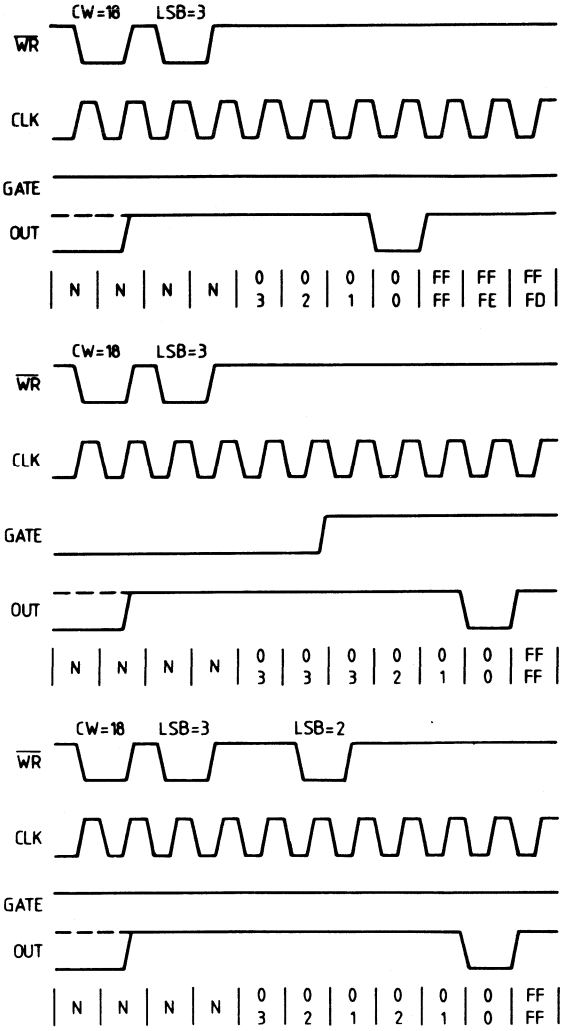
Note:
A GATE transition should not occur one clock prior to terminal count.

Mode 3 Timing Diagram



Note:
A GATE transition should not occur one clock prior to terminal count.

Mode 4 Timing Diagram



Mode 4: Software-Triggered Strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5: Hardware-Triggered Strobe (retriggerable)

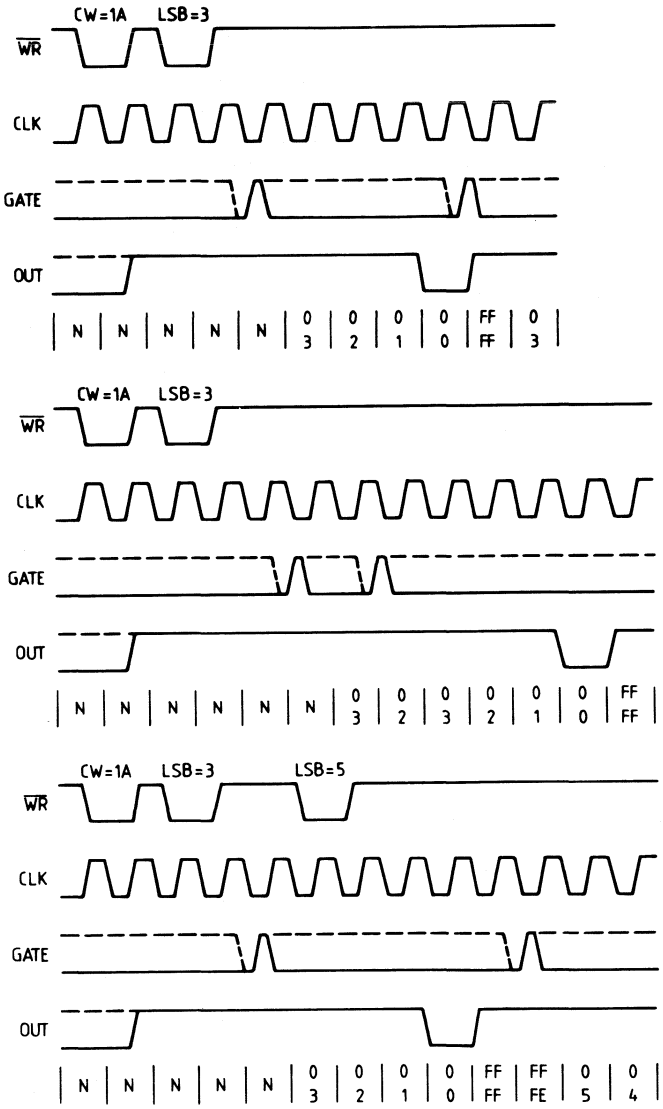
OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the control word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger results in the counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Mode 5 Timing Diagram



Operation Common to All Modes

Programming

When a control word is written to a counter, all control logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In modes 0, 2, 3, and 4 the GATE input is level-sensitive, and the logic level is sampled on the rising edge of CLK. In modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these modes a rising edge of GATE (trigger) sets an edge-sensitive flipflop in the counter. This flipflop is then sampled on the next rising edge of CLK; the flipflop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs – a high logic level does not have to be maintained until the next rising edge of CLK. Note that in modes 2 and 3, the GATE input is both edge- and level-sensitive. In modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

GATE Pin Operations Summary

Signal Status Modes	Low or Going Low	Rising	High
0	Disables Counting	–	Enables Counting
1	–	1) Initiates Counting 2) Resets Output after Next Clock	–
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	–	Enables Counting
5	–	Initiates Counting	–

Counter

New counts are loaded and counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In modes 0, 1, 4, and 5 the counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the counter reloads itself with the initial count and continues counting from there.

Minimum and Maximum Initial Counts

Mode	Min. Count	Max. Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

Note:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Absolute Maximum Ratings[1)]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to + 150°C
Supply voltage	−0.5 to + 8.0V
Voltage on any input	−2.0V to V_{CC} + 0.5V
Voltage on any output	−0.5V to V_{CC} + 0.5V
Power dissipation	1W

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input load current	–	±1	µA	$0 \leq V_{IN} \leq V_{CC}$
I_{OFL}	Output float leakage current	–	±10	µA	$0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	V_{CC} supply current	–	10	mA	f = max. CLK frequency $V_{IN} = V_{CC}$ or GND All outputs open
I_{CCSB}	V_{CC} supply current-standby	–	10	µA	f_C = 0 (DC) $\overline{CS}$ = 1 All inputs/data bus high All outputs floating

Capacitance[2)]

T_A = 25°C, V_{CC} = GND = 0V, f_C = 1 MHz

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	
C_{OUT}	Output capacitance	–	15	pF	

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) These parameters are periodically sampled, not 100% tested.

AC Characteristics SAB 82C53

T_A = 0 to 70°C, V_{CC} = 5 V ±10%
AC timings are referred to 0.8 and 2.0 V points of signals unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AR}	Address stable before $\overline{RD}\downarrow$	50	–	ns	–
t_{RA}	Address hold time after $\overline{RD}\downarrow$	5	–	ns	–
t_{RR}	$\overline{RD}$ pulse width	400	–	ns	–
t_{RD}	Data delay from $\overline{RD}\downarrow$	–	300	ns	–
t_{DF}	$\overline{RD}\uparrow$ to data floating	25	125	ns	–
t_{RV}	Command recovery time	1	–	µs	–
t_{AW}	Address stable before $\overline{WR}\downarrow$	50	–	ns	–
t_{WA}	Address hold time after $\overline{WR}\uparrow$	30	–	ns	–
t_{WW}	$\overline{WR}$ pulse width	400	–	ns	–
t_{DW}	Data setup time before $\overline{WR}\uparrow$	300	–	ns	–
t_{WD}	Data hold time after $\overline{WR}\uparrow$	40	–	ns	–
t_{RV}	Command recovery time	1	–	µs	–
t_{CLK}	Clock period	380	DC	ns	–
t_{PWH}	High pulse width	230	–	ns	[1]
t_{PWL}	Low pulse width	150	–	ns	[1]
t_{GW}	Gate width high	150	–	ns	–
t_{GL}	Gate width low	100	–	ns	–
t_{GS}	Gate setup time to CLK $\uparrow$	100	–	ns	–
t_{GH}	Gate hold time after CLK $\uparrow$	50	–	ns	[2]
t_{OD}	Output delay from CLK $\downarrow$	–	400	ns	–
t_{ODG}	Output delay from GATE $\downarrow$	–	300	ns	–

[1] Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
[2] In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns of the rising clock edge may not be detected.

AC Characteristics SAB 82C53-5

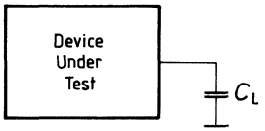
T_A = 0 to 70°C, V_{CC} = 5 V ±10%
AC timings are referred to 0.8 and 2.0 V points of signals unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AR}	Address stable before $\overline{RD}$ ↓	30	–	ns	–
t_{RA}	Address hold time after $\overline{RD}$ ↓	5	–	ns	–
t_{RR}	$\overline{RD}$ pulse width	300	–	ns	–
t_{RD}	Data delay from $\overline{RD}$ ↓	–	200	ns	–
t_{DF}	$\overline{RD}$ ↑ to data floating	25	100	ns	–
t_{RV}	Command recovery time	1	–	µs	–
t_{AW}	Address stable before $\overline{WR}$ ↓	30	–	ns	–
t_{WA}	Address hold time after $\overline{WR}$ ↑	30	–	ns	–
t_{WW}	$\overline{WR}$ pulse width	300	–	ns	–
t_{DW}	Data setup time before $\overline{WR}$ ↑	250	–	ns	–
t_{WD}	Data hold time after $\overline{WR}$ ↑	30	–	ns	–
t_{RV}	Command recovery time	1	–	µs	–
t_{CLK}	Clock period	380	DC	ns	–
t_{PWH}	High pulse width	230	–	ns	[1]
t_{PWL}	Low pulse width	150	–	ns	[1]
t_{GW}	Gate width high	150	–	ns	–
t_{GL}	Gate width low	100	–	ns	–
t_{GS}	Gate setup time to CLK ↑	100	–	ns	–
t_{GH}	Gate hold time after CLK ↑	50	–	ns	[2]
t_{OD}	Output delay from CLK ↓	–	400	ns	–
t_{ODG}	Output delay from GATE ↓	–	300	ns	–

[1] Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
[2] In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 70 ns of the rising clock edge may not be detected.

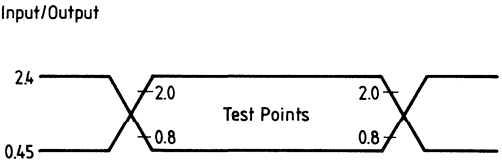
AC Testing Waveforms

Test Loadings



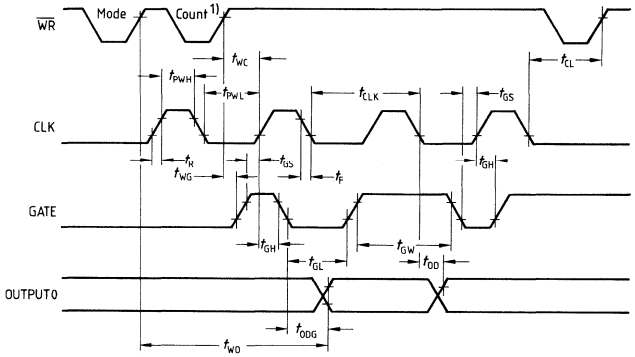
C_L = 150 pF
C_L Includes Jig Capacitance

Measurement Reference Levels



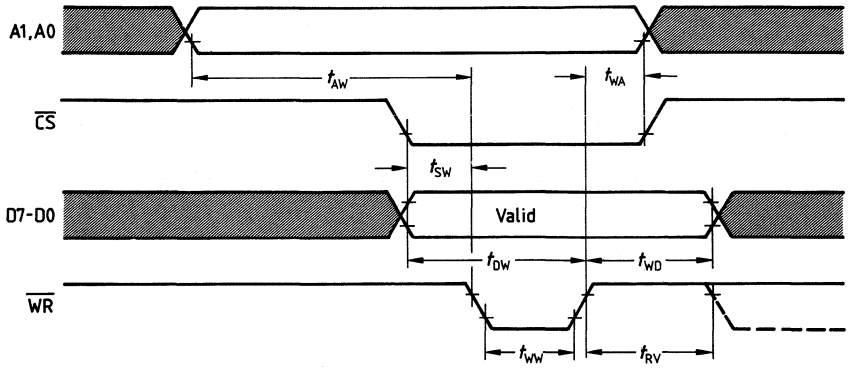
AC Testing: Inputs are driven at 2.4V for a logic "1" and at 0.45V for a logic "0".

Counter Control Timing

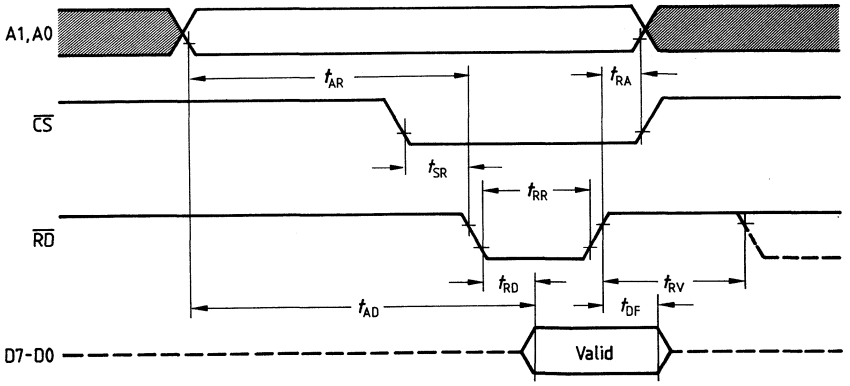


1) Last byte of count being written

Write Cycle Timing

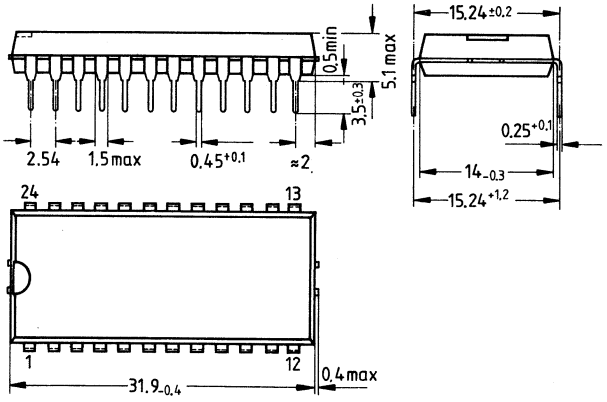


Read Cycle Timing



Package Outlines

Plastic Package, P-DIP-24
(dual-in-line package)



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 82C53-P	Q67120-P217	Programmable CMOS interval timer
SAB 82C53-5-P	Q67120-P264	Programmable CMOS interval timer

Preliminary

SAB 82C54 Programmable CMOS Interval Timer

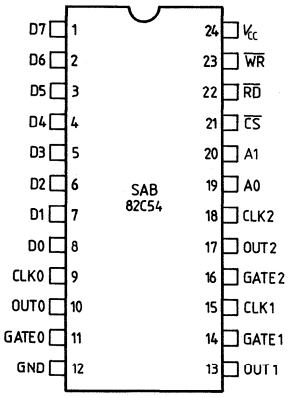
SAB 82C54 up to 8 MHz

- Compatible with all Siemens and most other microprocessors
- Three independent 16-bit counters
- Handles inputs from DC to 8 MHz (10 MHz for SAB 82C54-1)

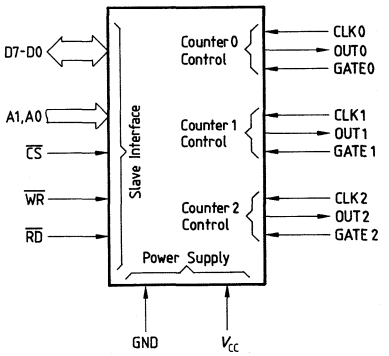
SAB 82C54-1 up to 10 MHz

- Low power CMOS (I_{CC} = 10 mA at max. count frequency)
- Completely TTL compatible
- Six programmable counter modes
- Binary or BCD counting
- Status read back command

Pin Configuration



Logic Symbol



The SAB 82C54 is a high-performance, CMOS version of the industry standard 8254 timer/counter which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software-programmable. The SAB 82C54 is pin-compatible with the NMOS 8254, and is a superset of the SAB 82C53.

Six programmable timer modes allow the SAB 82C54 to be used as an event counter, elapsed time indicator, programmable monoflop, and in many other applications.

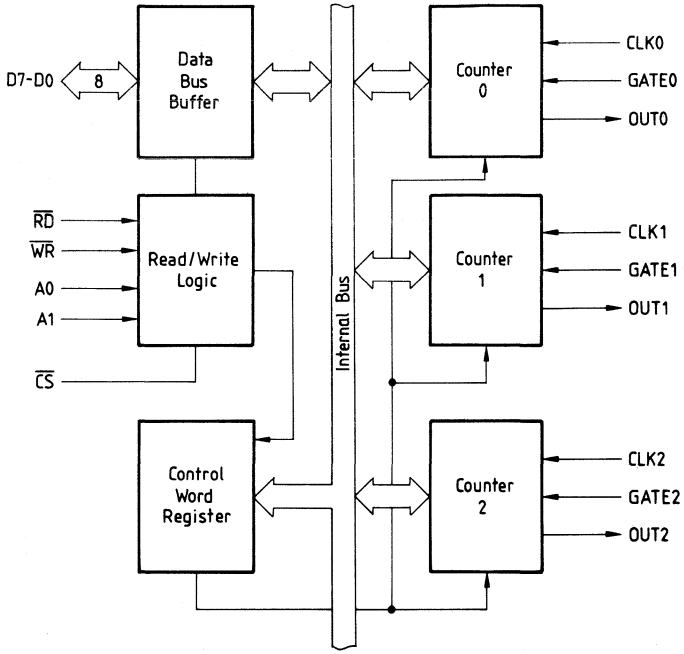
The SAB 82C54 is fabricated in Siemens advanced CMOS technology which provides low power consumption and is packaged in a 24-pin dual-in-line package.

9.87

Pin Definitions and Functions

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>D7-D0</td><td>1-8</td><td>I/O</td><td>DATA 7-0
Bidirectional tristate data bus lines, connected to system data bus.</td></tr>
<tr><td>CLK 0</td><td>9</td><td>I</td><td>CLOCK 0
Clock input of counter 0.</td></tr>
<tr><td>OUT 0</td><td>10</td><td>O</td><td>OUTPUT 0
Output of counter 0.</td></tr>
<tr><td>GATE 0</td><td>11</td><td>I</td><td>GATE 0
Gate input of counter 0.</td></tr>
<tr><td>OUT 1</td><td>13</td><td>O</td><td>OUTPUT 1
Output of counter 1.</td></tr>
<tr><td>GATE 1</td><td>14</td><td>I</td><td>GATE 1
Gate input of counter 1.</td></tr>
<tr><td>CLK 1</td><td>15</td><td>I</td><td>CLOCK 1
Clock input of counter 1.</td></tr>
<tr><td>GATE 2</td><td>16</td><td>I</td><td>GATE 2
Gate input of counter 2.</td></tr>
<tr><td>OUT 2</td><td>17</td><td>O</td><td>OUTPUT 2
Output of counter 2.</td></tr>
<tr><td>CLK 2</td><td>18</td><td>I</td><td>CLOCK 2
Clock input of counter 2.</td></tr>
<tr><td>A1, A0</td><td>20-19</td><td>I</td><td>ADDRESS 1, 0
Used to select one of the three counters or the control word register for read or write operations. Normally connected to the system address bus.
<table>
<tr><th>A1</th><th>A0</th><th>Selects</th></tr>
<tr><td>0</td><td>0</td><td>Counter 0</td></tr>
<tr><td>0</td><td>1</td><td>Counter 1</td></tr>
<tr><td>1</td><td>0</td><td>Counter 2</td></tr>
<tr><td>1</td><td>1</td><td>Control Word Register</td></tr>
</table></td></tr>
<tr><td>$\overline{CS}$</td><td>21</td><td>I</td><td>$\overline{CHIP\ SELECT}$
A low on this input enables the SAB 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.</td></tr>
<tr><td>$\overline{RD}$</td><td>22</td><td>I</td><td>$\overline{READ\ CONTROL}$
This input is low during CPU read operations.</td></tr>
<tr><td>$\overline{WR}$</td><td>23</td><td>I</td><td>$\overline{WRITE\ CONTROL}$
This input is low during CPU write operations.</td></tr>
<tr><td>V_{CC}</td><td>24</td><td>–</td><td>POWER SUPPLY (+5V)</td></tr>
<tr><td>GND</td><td>12</td><td>–</td><td>GROUND (0 V)</td></tr>
</table>

Block Diagram



Functional Description

General

The SAB 82C54 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general-purpose, multitiming element that can be treated as an array of I/O ports in the system software.

The SAB 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the SAB 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the SAB 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other timer/counter functions common to microcomputers which can be implemented with the SAB 82C54 are:

- Real time clock
- Event counter
- Digital monoflop
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Slave Interface

The bidirectional tristate data bus buffer is used to interface the SAB 82C54 to the system bus.

The read/write logic accepts inputs from the system bus and generates control signals for the other functional blocks of the SAB 82C54. A1 and A0 select one of the three counters or the control word register for read or write accesses. An active (low) $\overline{RD}$ input allows the CPU to read one of the counters. An active (low) $\overline{WR}$ input allows the CPU to write into one of the control word registers. $\overline{RD}$ and $\overline{WR}$ are ignored unless the SAB 82C54 is selected by an active (low) $\overline{CS}$ input.

Control Word Register

The control word register is selected by the read/write logic with A1, A0 = 11. A CPU write operation stores a control word into the control word register. These control words specify the operating mode of the counters.

The control word register can only be written to; status information is available with the read-back command.

Counters

These three functional blocks are identical in operation, so only a single counter will be described.

The counters are fully independent. Each counter may operate in a different mode. The internal block diagram of a single counter is shown in the following figure. The control word register shown in the figure is not part of the counter itself, but determines the operating mode of the counter.

The status register, shown in the figure, when latched, contains the current contents of the control word register and status of the output and null count flag. (See detailed explanation of the read-back command.)

The actual counter is labelled CE (for "counting element"). It is a 16-bit presettable synchronous down counter.

Output latch M and output latch L are two 8-bit latches. The designations M and L stand for "most significant byte" and "least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable counter latch command is sent to the SAB 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's control logic to drive the internal bus. This is how the 16-bit counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called count register M and count register L. Both are normally referred to as one unit and called just CR. When a new count is written to the counter, the count is stored in the CR and later transferred to the CE. The control logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR M and CR I are cleared when the counter is programmed. In this way, if the counter has been programmed for one byte counts (either most significant byte only or least significant byte only), the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

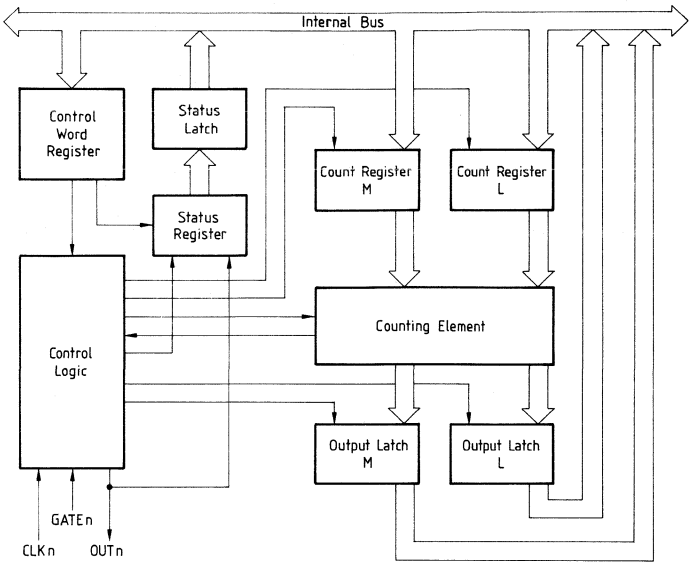
The control logic is also shown in the diagram. CLKn, GATEn, and OUTn are all connected to the outside world through the control logic.

System Interface

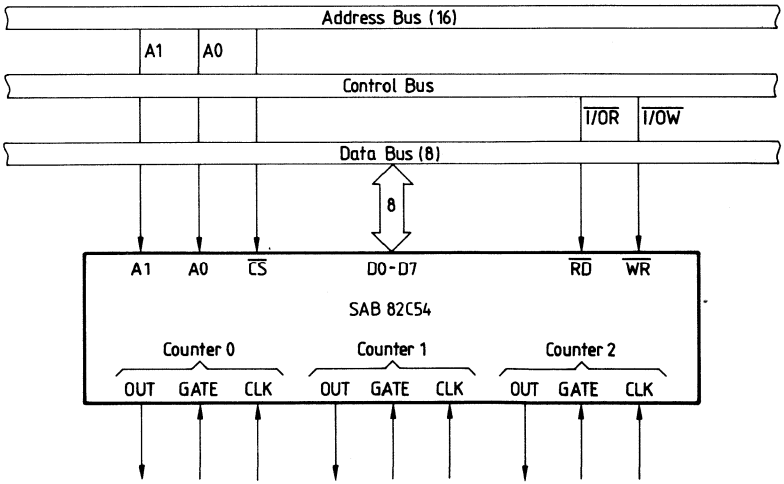
The SAB 82C54 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for mode programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder for larger systems.

Internal Block Diagram of a Counter



SAB 82C54 System Interface



Operational Description

General

After power-up, the state of the SAB 82C54 is undefined. The mode, count value, and output of all counters are undefined.

The operating mode of each counter is determined when it is programmed. Each counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the SAB 82C54

Counters are programmed by writing a control word and then an initial count. The control word format is shown in the following figure.

All control words are written into the control word register, which is selected with A1, A0 = 11. The control word itself specifies which counter is being programmed.

By contrast, initial counts are written into the counters, not the control word register. The A1, A0 inputs are used to select the counter to be written into. The format of the initial count is determined by the control word used.

Control Word Format

A1, A0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see read operations)

RW – Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see read operations)
0	1	Read/Write Least Significant Byte Only.
1	0	Read/Write Most Significant Byte Only.
1	1	Read/Write Least Significant Byte First, Then Most Significant Byte.

M – Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter, 16-Bit
1	Binary-Coded Decimal (BCD) Counter (4 decades)

NOTE: Don't care bits (X) should be 0 to insure compatibility with future products.

Write Operations

The programming procedure for the SAB 82C54 is very flexible. Only two conventions need to be remembered:

1) For each counter the control word must be written before the initial count is written.
2) The initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the control word register and the three counters have separate addresses (selected by the A1, A0 inputs), and each control word specifies the counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a counter at any time without affecting the counter's programmed mode in any way. Counting will be affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

A Few Possible Programming Sequences

	A1	A0
Control Word – Counter 0	1	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0
Control Word – Counter 1	1	1
LSB of Count – Counter 1	0	1
MSB of Count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 2	1	0

	A1	A0
Control Word – Counter 2	1	1
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 2	1	0
LSB of Count – Counter 1	0	1
MSB of Count – Counter 1	0	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0

	A1	A0
Control Word – Counter 0	1	1
Counter Word – Counter 1	1	1
Control Word – Counter 2	1	1
LSB of Count – Counter 2	1	0
LSB of Count – Counter 1	0	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0
MSB of Count – Counter 1	0	1
MSB of Count – Counter 2	1	0

	A1	A0
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of Count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 1	0	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 0	0	0
MSB of Count – Counter 2	1	0

Note:
In all four examples, all counters are programmed to read/write two-byte counts.
These are only four of many possible programming sequences.

Read Operations

It is often desirable to read the value of a counter without disturbing the count in progress. This is easily done in the SAB 82C54.

There are three possible methods for reading the counters: a simple read operation, the counter latch command, and the read-back command.

Each is explained below. The first method is to perform a simple read operation. To read the counter which is selected with the A1, A0 inputs, the CLK input of the selected counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

Counter Latch Command

The second method uses the "counter latch command". Like a control word, this command is written to the control word register, which is selected with A1, A0 = 11. Also like a control word, the SC0, SC1 bits select one of the three counters, but two other bits, D5 and D4, distinguish this command from a control word.

The selected counter's output latch (OL) latches the count at the time the counter latch command is received. This count is held in the latch until it is read by the CPU (or until the counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the counters "on the fly" without affecting counting in progress. Multiple counter latch commands may be used to latch more than one counter. Each latched counter's OL holds its count until it is read. Counter latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second counter latch command is ignored. The count read will be the count at the time the first counter latch command was issued.

With either method, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other counters may be inserted between them.

Another feature of the SAB 82C54 is that reads and writes of the same counter may be interleaved; for example, if the counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte
2. Write new least significant byte
3. Read most significant byte
4. Write new most significant byte

If a counter is programmed to read/write two-byte counts, the following precaution applies; a program must not transfer control between reading the first and second byte to another routine which also reads from that same counter. Otherwise, an incorrect count will be read.

Counter Latch Command Format

A1, A0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 = specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-back command

D5, D4 = 00 designates counter latch command

X = don't care

Note:
Don't care bits (X) should be 0 to insure compatibility with future products.

Read-Back Command

The third method uses the read-back command. This command allows the user to check the count value, programmed mode, current state of the OUT pin, and "null count" flag of the selected counter(s).

The command is written into the control word register and has the format shown in the figure below. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 to 1.

The read-back command may be used to latch multiple counter output latches (OL) by setting the $\overline{COUNT}$ bit D5 to 0 and selecting the desired counter(s). The single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the

Read-Back Command Format

A0, A1 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT2	CNT1	CNT0	0

D5: 0 = Latch Count of Selected Counter(s)
D4: 0 = Latch Status of Selected Counter(s)
D3: 1 = Select Counter 2
D2: 1 = Select Counter 1
D1: 1 = Select Counter 0
D0: Reserved for Future Expansion; Must Be 0

Status Byte

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7: 1 = OUT Pin is 1
0 = OUT Pin is 0
D6: 1 = Null count
0 = Count available for reading
D5-D0: Counter programmed mode

count, all but the first are ignored, i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting $\overline{\text{STATUS}}$ bit D4 to 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in the next figure. Bits D5 through D0 contain the counter's programmed mode exactly as written in the last mode control word. Output bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

Null count bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time when this happens depends on the mode of the counter and is described in the mode definitions, but until the count is loaded into the counting element (CE), it cannot be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of null count is shown in the following figure.

Null Count Operation

THIS ACTION:	CAUSES:
A. Write to the control word register: [1]	Null count = 1
B. Write to the count register (CR); [2]	Null count = 1
C. New count is loaded into CE (CR → CE);	Null count = 0

[1] Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

[2] If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ bits D5, D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in the figure below.

If both count and status of a counter are latched, the first read operation of that counter will return the latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two byte counts) return latched count. Subsequent reads return unlatched count.

Read-Back Command Example

Command								Description	Results
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read Back Count and Status of Counter 0	Count and Status Latched for Counter 0
1	1	1	0	0	1	0	0	Read Back Status of Counter 1	Status Latched for Counter 1
1	1	1	0	1	1	0	0	Read Back Status of Counter 2, 1	Status Latched for Counter 2, but Not Counter 1
1	1	0	1	1	0	0	0	Read Back Count of Counter 2	Count Latched for Counter 2
1	1	0	0	0	1	0	0	Read Back Count and Status of Counter 1	Count Latched for Counter 1, but Not Status
1	1	1	0	0	0	1	0	Read Back Status of Counter 1	Command Ignored, Status Already Latched for Counter 1

Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Description
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No Operation (tristate)
1	X	X	X	X	No Operation (tristate)
0	1	1	X	X	No Operation (tristate)

Mode Definitions

The following are defined for use in describing the operation of the SAB 82C54.

CLK pulse: a rising edge, then a falling edge, in that order, of a counter's CLK input.

Trigger: a rising edge of a counter's GATE input.

Counter loading: the transfer of a count from the CR to the CE (refer to the "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the control word is written, OUT is initially low, and will remain low until the counter reaches zero. OUT then goes high and remains high until a new count or a new mode 0 control word is written into the counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the control word and initial count are written to a counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

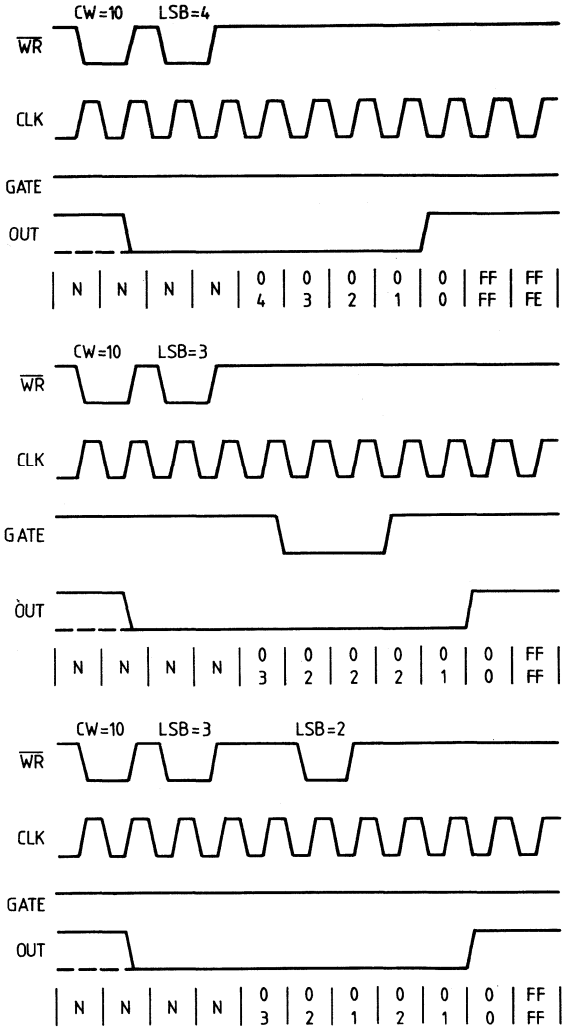
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

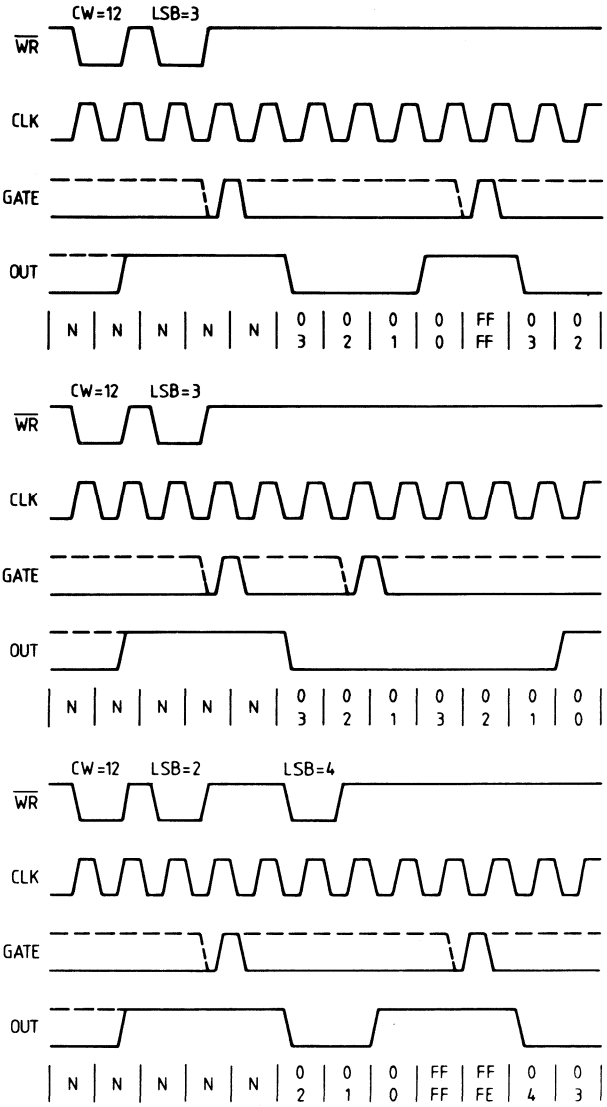
If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

Note:
The following conventions apply to all Mode Timing Diagrams:
1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant bytes (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "control word"; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values.
The lower number is the least significant byte.
The upper number is the most significant byte.
Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Mode 0 Timing Diagram



Mode 1 Timing Diagram



Mode 1: Hardware-Retriggerable Single-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the single-shot pulse, and will remain low until the counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the control word and initial count, the counter is armed. A trigger results in loading the counter and setting OUT low on the next CLK pulse, thus starting the single-shot pulse. An initial count of N will result in a single-shot pulse N CLK cycles in duration. The single-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The single-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the counter during a single-shot pulse, the current single-shot is not affected unless the counter is retriggered. In that case, the counter is loaded with the new count and the pulse continues until the new count expires.

Mode 2: Rate Generator

This mode functions like a divide-by-N counter. It is typically used to generate a real-time clock interrupt. OUT will initially be high. When the initial count has decrement to 1, OUT goes low for one CLK pulse. OUT then goes high again, the counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated infinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the counter.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

Mode 3: Square Wave Mode

Mode 3 is typically used for baud rate generation. Mode 3 is similar to mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated infinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the counter.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This allows the counter to be synchronized by software also.

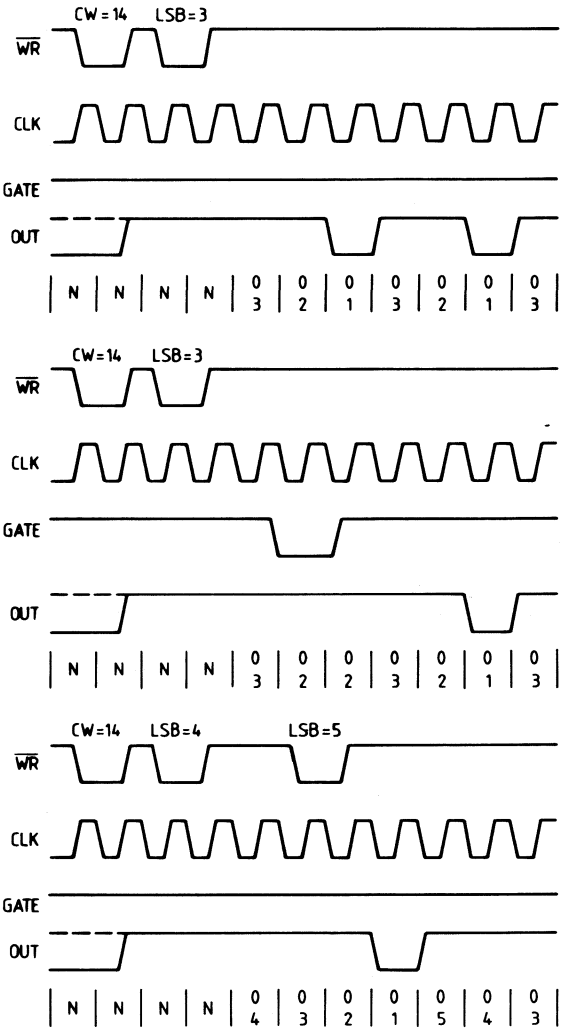
Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the counter is reloaded with the initial count. The above process is repeated infinitely.

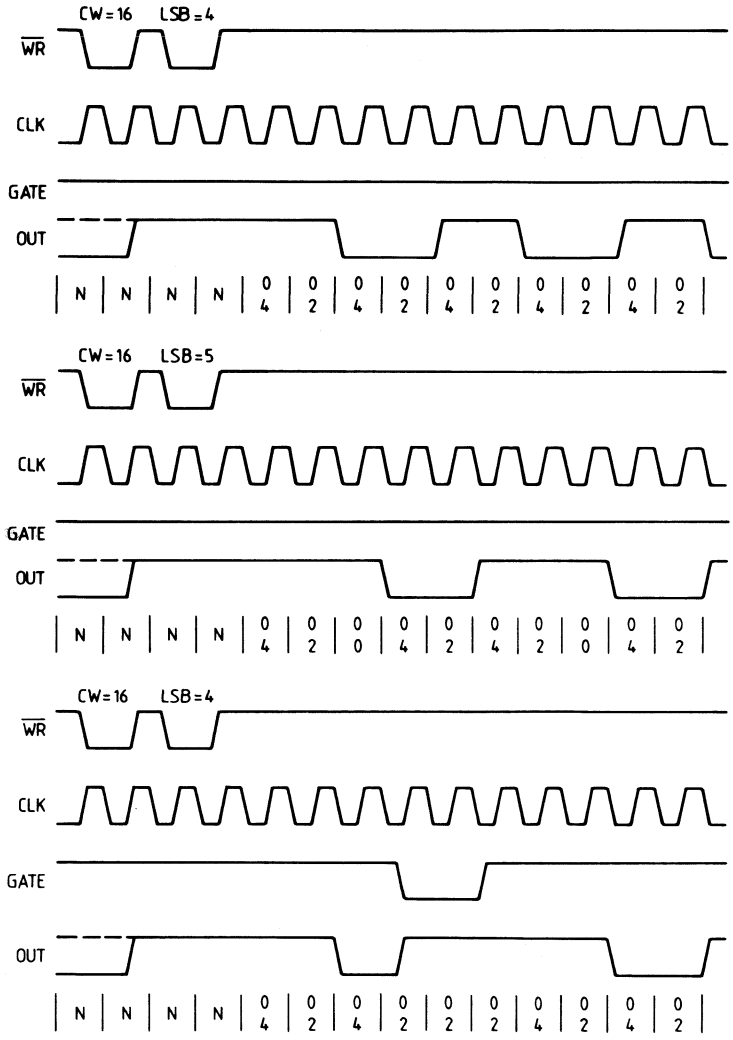
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the counter is reloaded with the initial count minus one. The above process is repeated infinitely. So for odd counts, OUT will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

Mode 2 Timing Diagram



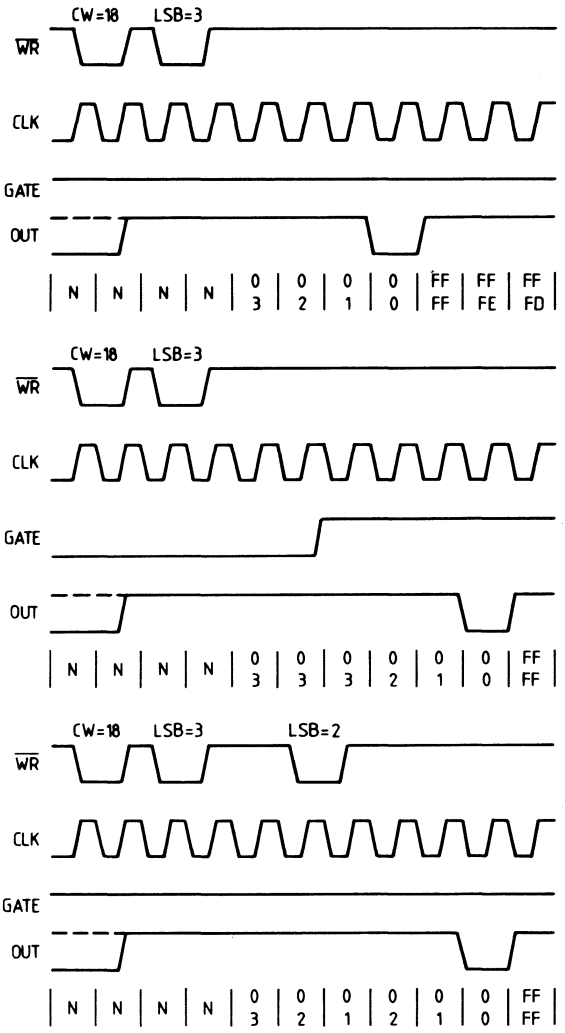
Note:
A GATE transition should not occur one clock prior to terminal count.

Mode 3 Timing Diagram



Note:
A GATE transition should not occur one clock prior to terminal count.

Mode 4 Timing Diagram



Mode 4: Software-Triggered Strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5: Hardware-Triggered Strobe (retriggerable)

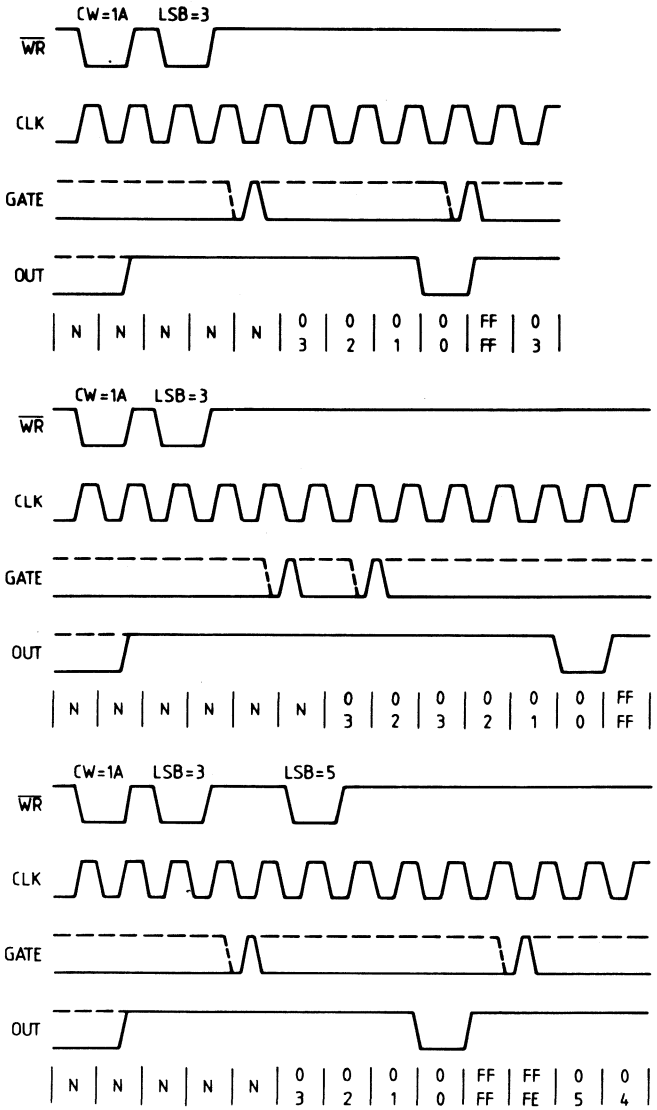
OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the control word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger results in the counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Mode 5 Timing Diagram



Operation Common to All Modes

Programming

When a control word is written to a counter, all control logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In modes 0, 2, 3, and 4 the GATE input is level-sensitive, and the logic level is sampled on the rising edge of CLK. In modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these modes a rising edge of GATE (trigger) sets an edge-sensitive flipflop in the counter. This flipflop is then sampled on the next rising edge of CLK; the flipflop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs – a high logic level does not have to be maintained until the next rising edge of CLK. Note that in modes 2 and 3, the GATE input is both edge- and level-sensitive. In modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

GATE Pin Operations Summary

Signal Status Modes	Low or Going Low	Rising	High
0	Disables Counting	–	Enables Counting
1	–	1) Initiates Counting 2) Resets Output after Next Clock	–
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	–	Enables Counting
5	–	Initiates Counting	–

Counter

New counts are loaded and counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In modes 0, 1, 4, and 5 the counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the counter reloads itself with the initial count and continues counting from there.

Minimum and Maximum Initial Counts

Mode	Min. Count	Max. Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

Note:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Absolute Maximum Ratings[1)]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to + 150°C
Supply voltage	−0.5 to + 8.0V
Voltage on any input	−2.0V to V_{CC} + 0.5V
Voltage on any output	−0.5V to V_{CC} + 0.5V
Power dissipation	1W

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input load current	–	±1	µA	$0 \leq V_{IN} \leq V_{CC}$
I_{OFL}	Output float leakage current	–	±10	µA	$0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	V_{CC} supply current	–	10	mA	f = max. CLK frequency $V_{IN} = V_{CC}$ or GND All outputs open
I_{CCSB}	V_{CC} supply current-standby	–	10	µA	f_C = 0 (DC) $\overline{CS}$ = 1 All inputs/data bus high All outputs floating

Capacitance[2)]

T_A = 25°C, V_{CC} = GND = 0V, f_C = 1 MHz

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	
C_{OUT}	Output capacitance	–	15	pF	

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) These parameters are periodically sampled, not 100% tested.

AC Characteristics SAB 82C54

T_A = 0 to 70°C, V_{CC} = 5 V ±10%
AC timings are referred to 0.8 and 2.0 V points of signals unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AR}	Address stable before $\overline{RD}$ ↓	45	–	ns	–
t_{SR}	$\overline{CS}$ stable before $\overline{RD}$ ↓	0	–	ns	–
t_{RA}	Address hold time after $\overline{RD}$ ↓	0	–	ns	–
t_{RR}	$\overline{RD}$ pulse width	150	–	ns	–
t_{RD}	Data delay from $\overline{RD}$ ↓	–	120	ns	–
t_{AD}	Data delay from address	–	220	ns	–
t_{DF}	$\overline{RD}$ ↑ to data floating	5	90	ns	–
t_{RV}	Command recovery time	200	–	ns	–
t_{AW}	Address stable before $\overline{WR}$ ↓	0	–	ns	–
t_{SW}	$\overline{CS}$ stable before $\overline{WR}$ ↓	0	–	ns	–
t_{WA}	Address hold time after $\overline{WR}$ ↑	0	–	ns	–
t_{WW}	$\overline{WR}$ pulse width	150	–	ns	–
t_{DW}	Data setup time before $\overline{WR}$ ↑	100	–	ns	–
t_{WD}	Data hold time after $\overline{WR}$ ↑	0	–	ns	–
t_{RV}	Command recovery time	200	–	ns	–
t_{CLK}	Clock period	125	DC	ns	–
t_{PWH}	High pulse width	60	–	ns	[1]
t_{PWL}	Low pulse width	60	–	ns	[1]
t_R	Clock rise time	–	100	ns	–
t_F	Clock fall time	–	100	ns	–
t_{GW}	Gate width high	50	–	ns	–
t_{GL}	Gate width low	50	–	ns	–
t_{GS}	Gate setup time to CLK ↑	50	–	ns	–
t_{GH}	Gate hold time after CLK ↑	50	–	ns	[2]
t_{OD}	Output delay from CLK ↓	–	150	ns	–
t_{ODG}	Output delay from GATE ↓	–	120	ns	–
t_{WC}	CLK delay for loading	0	55	ns	–
t_{WG}	Gate delay for sampling	−5	50	ns	–
t_{WO}	OUT delay from mode write	–	260	ns	–
t_{CL}	CLK setup for count latch	−4	45	ns	–

[1] Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
[2] In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns of the rising clock edge may not be detected.

AC Characteristics SAB 82C54-1

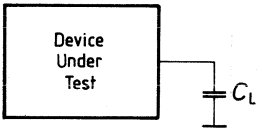
T_A = 0 to 70°C, V_{CC} = 5 V ±10%
AC timings are referred to 0.8 and 2.0 V points of signals unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AR}	Address stable before $\overline{RD}$ ↓	30	–	ns	–
t_{SR}	$\overline{CS}$ stable before $\overline{RD}$ ↓	0	–	ns	–
t_{RA}	Address hold time after $\overline{RD}$ ↓	0	–	ns	–
t_{RR}	$\overline{RD}$ pulse width	95	–	ns	–
t_{RD}	Data delay from $\overline{RD}$ ↓	–	85	ns	–
t_{AD}	Data delay from address	–	185	ns	–
t_{DF}	$\overline{RD}$ ↑ to data floating	5	65	ns	–
t_{RV}	Command recovery time	165	–	ns	–
t_{AW}	Address stable before $\overline{WR}$ ↓	0	–	ns	–
t_{SW}	$\overline{CS}$ stable before $\overline{WR}$ ↓	0	–	ns	–
t_{WA}	Address hold time after $\overline{WR}$ ↑	0	–	ns	–
t_{WW}	$\overline{WR}$ pulse width	95	–	ns	–
t_{DW}	Data setup time before $\overline{WR}$ ↑	85	–	ns	–
t_{WD}	Data hold time after $\overline{WR}$ ↑	0	–	ns	–
t_{RV}	Command recovery time	165	–	ns	–
t_{CLK}	Clock period	100	DC	ns	–
t_{PWH}	High pulse width	30	–	ns	[1]
t_{PWL}	Low pulse width	50	–	ns	[1]
t_R	Clock rise time	–	100	ns	–
t_F	Clock fall time	–	100	ns	–
t_{GW}	Gate width high	50	–	ns	–
t_{GL}	Gate width low	50	–	ns	–
t_{GS}	Gate setup time to CLK ↑	40	–	ns	–
t_{GH}	Gate hold time after CLK ↑	50	–	ns	[2]
t_{OD}	Output delay from CLK ↓	–	100	ns	–
t_{ODG}	Output delay from GATE ↓	–	100	ns	–
t_{WC}	CLK delay for loading	0	55	ns	–
t_{WG}	Gate delay for sampling	−5	40	ns	–
t_{WO}	OUT delay from mode write	–	240	ns	–
t_{CL}	CLK setup for count latch	−4	40	ns	–

[1] Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
[2] In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 70 ns of the rising clock edge may not be detected.

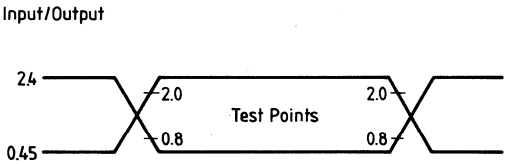
AC Testing Waveforms

Test Loadings



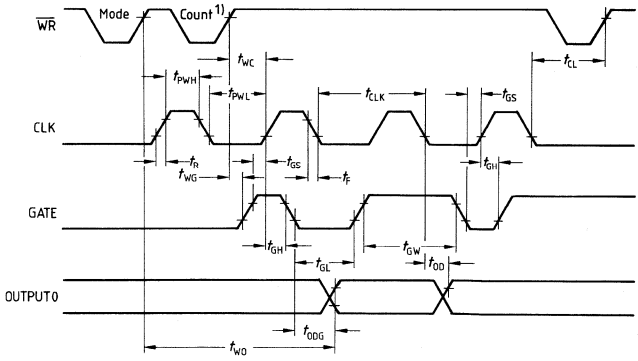
C_L = 150 pF
C_L Includes Jig Capacitance

Measurement Reference Levels



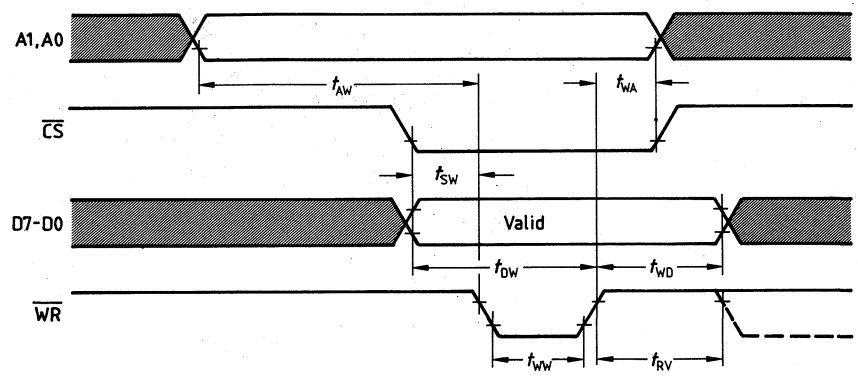
AC Testing: Inputs are driven at 2.4V for a logic "1" and at 0.45V for a logic "0".

Counter Control Timing

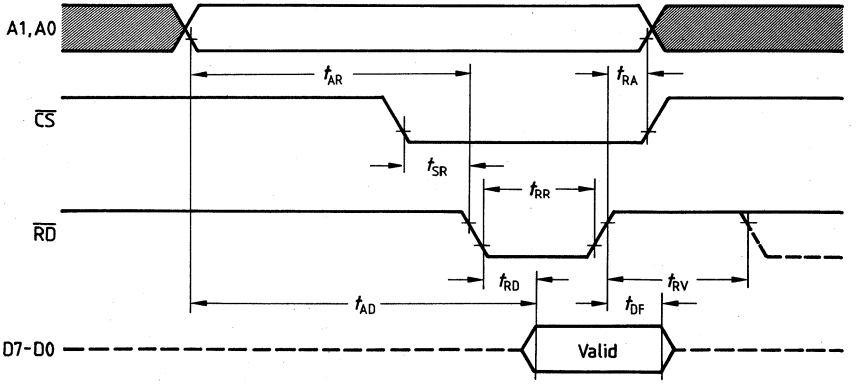


1) Last byte of count being written

Write Cycle Timing

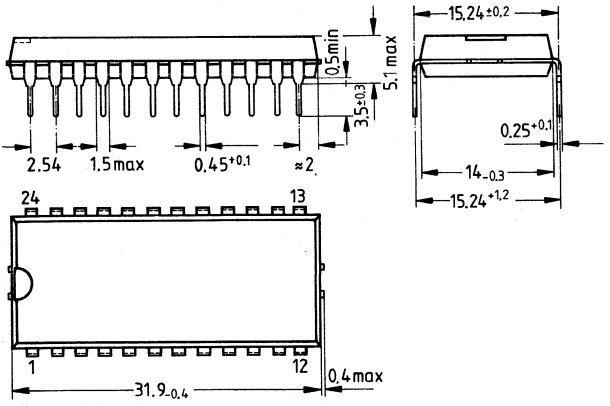


Read Cycle Timing



Package Outlines

Plastic Package, P-DIP-24
(dual-in-line package)
20 B 24 DIN 41870 T 10



Dimensions in mm

Ordering Information

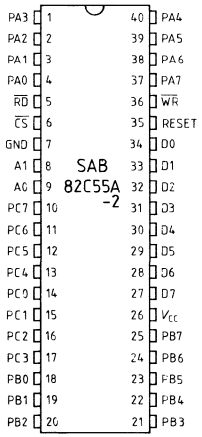
Type	Ordering code	Description
SAB 82C54-P	Q67120-P212	Programmable CMOS interval timer
SAB 82C54-1-P	Q67120-P237	Programmable CMOS interval timer

Preliminary

SAB 82C55A-2 CMOS Programmable Peripheral Interface

- Compatible with all Siemens and most other microprocessors
- High-speed "zero wait state" operation with 8 MHz SAB 8086/8088 and SAB 80186/80188
- 24 programmable I/O pins
- Low-power CMOS
- Completely TTL-compatible
- Control word read-back capability
- Direct bit-set/reset capability
- 2.5 mA DC drive capability on all I/O port outputs
- Available in 40-pin dual-in-line package

Figure 1
Pin Configuration



Pin Names

PA 3-0	Port A, Pins 0 to 3
$\overline{RD}$	Read Input
$\overline{CS}$	Chip Select
A 1-0	Address Inputs
PC 7-4	Port C, Pins 4 to 7
PC 0-3	Port C, Pins 0 to 3
PB 0-7	Port B, Pins 0 to 7
D 7-0	Data Bus (bidirectional)
RESET	Reset Input
$\overline{WR}$	Write Input
PA 7-4	Port A, Pins 4 to 7

The SAB 82C55A-2 is a high-performance, CMOS version of the industry standard 8255A general-purpose, programmable I/O device which is designed for use with all Siemens and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12, and used in 3 major modes of operation. The SAB 82C55A-2 is pin-compatible with the NMOS 8255A and 8255A-5.

In mode 0 , each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In mode 1, each group may be programmed to have 8 lines of input or output. Three of the remaining 4 pins are used for handshaking and interrupt control signals. Mode 2 is a strobed bidirectional bus configuration.

The SAB 82C55A-2 is fabricated in Siemens CMOS technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The SAB 82C55A-2 is available in a 40-pin dual-in-line package.

9.87

Pin Definitions and Functions

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>PA3-PA0</td><td>1-4</td><td>I/O</td><td>PORT A, PINS 0–3
Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.</td></tr>
<tr><td>$\overline{RD}$</td><td>5</td><td>I</td><td>$\overline{READ\ CONTROL}$
This input is low during CPU read operations.</td></tr>
<tr><td>$\overline{CS}$</td><td>6</td><td>I</td><td>$\overline{CHIP\ SELECT}$
A low on this input enables the SAB 82C55A-2 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.</td></tr>
<tr><td>A1-A0</td><td>8-9</td><td>I</td><td>ADDRESS INPUTS 1 AND 0
These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one the three ports or of the control word registers.
<table>
<tr><th>A1</th><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Input Operation (read)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port A - Data Bus</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Port B - Data Bus</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port C - Data Bus</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Control Word - Data Bus</td></tr>
<tr><td colspan="5"></td><td>Output Operation (write)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port A</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port B</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port C</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Control</td></tr>
<tr><td colspan="5"></td><td>Disable Function</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>Data Bus - Tristate</td></tr>
<tr><td>X</td><td>X</td><td>1</td><td>1</td><td>0</td><td>Data Bus - Tristate</td></tr>
</table></td></tr>
<tr><td>PC7-PC4</td><td>10-13</td><td>I/O</td><td>PORT C, PINS 4-7
Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch, and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.</td></tr>
<tr><td>PC0-PC3</td><td>14-17</td><td>I/O</td><td>PORT C, PINS 0-3
Lower nibble of port C.</td></tr>
<tr><td>PB0-PB7</td><td>18-25</td><td>I/O</td><td>PORT B, PINS 0-7
An 8-bit data output latch/buffer and an 8-bit data input buffer.</td></tr>
</table>

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
D7-D0	27-34	I/O	DATA BUS Bidirectional, tristate data bus lines, connected to system data bus.
RESET	35	I	RESET A high on this input clears the control register and all ports are set to the input mode.
$\overline{WR}$	36	I	$\overline{WRITE\ CONTROL}$ This input is low during CPU write operations.
PA7-PA4	37-40	I/O	PORT A, PINS 4-7 Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.
V_{CC}	26	–	POWER SUPPLY (+5V)
GND	7	–	SYSTEM GROUND (0V)

Functional Description

General

The SAB 82C55A-2 is a programmable peripheral interface device designed for use in Siemens microcomputer systems. Its function is that of a general-purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the SAB 82C55A-2 is programmed by system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This tristate bidirectional 8-bit buffer is used to interface the SAB 82C55A-2 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both data and control or status words. It accepts inputs from the CPU address and control buses and, in turn, issues commands to both of the control groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the SAB 82C55A-2. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the SAB 82C55A-2.

Each of the control blocks (group A and group B) accepts "commands" from the read/write control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control group A - port A and upper port C (C7-C4)
Control group B - port B and lower port C (C3-C0)

The control word register can be both written and read as shown in the address decode table in the pin description. Figure 5 shows the control word format for both read and write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The SAB 82C55A-2 contains three 8-bit ports (A, B, and C). All of them can be configured in a wide variety of functional characteristics by the system software, but each has its own special features or "personality" to further enhance the power and flexibility of the SAB 82C55A-2.

Port A One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pullup" and "pulldown" bus-hold devices are present on port A.

Port B One 8-bit data input/output latch/buffer. Only "pullup" bus-hold devices are present on port B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pullup" bus-hold devices are present on port C.

See figure 3 for the bus-hold circuit configuration for ports A, B, and C.

Figure 2
Block Diagram

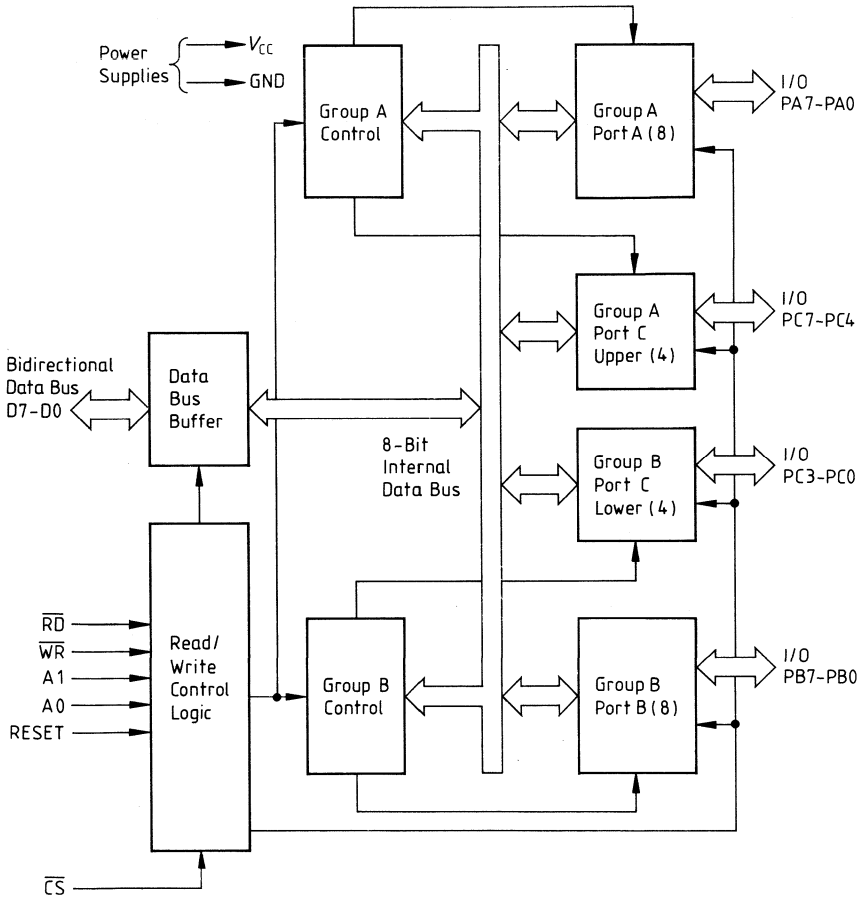
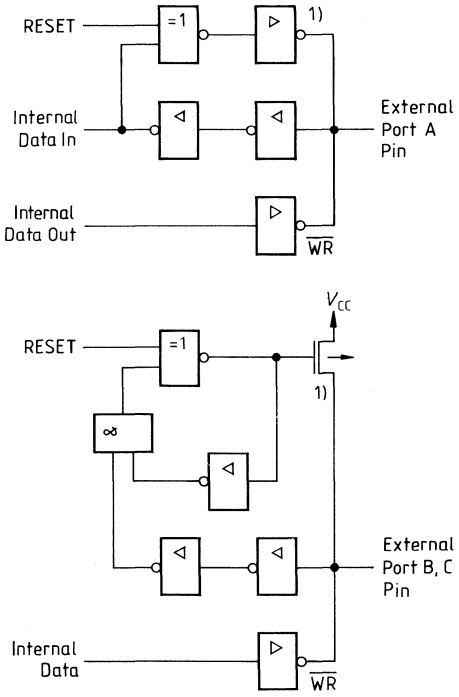


Figure 3
Port A, B, C, Bus-Hold Configuration



[1]) Port pins loaded with more than 20 pF capacitance may not have their logic level guaranteed following a hardware reset.

Operational Description

Mode Selection

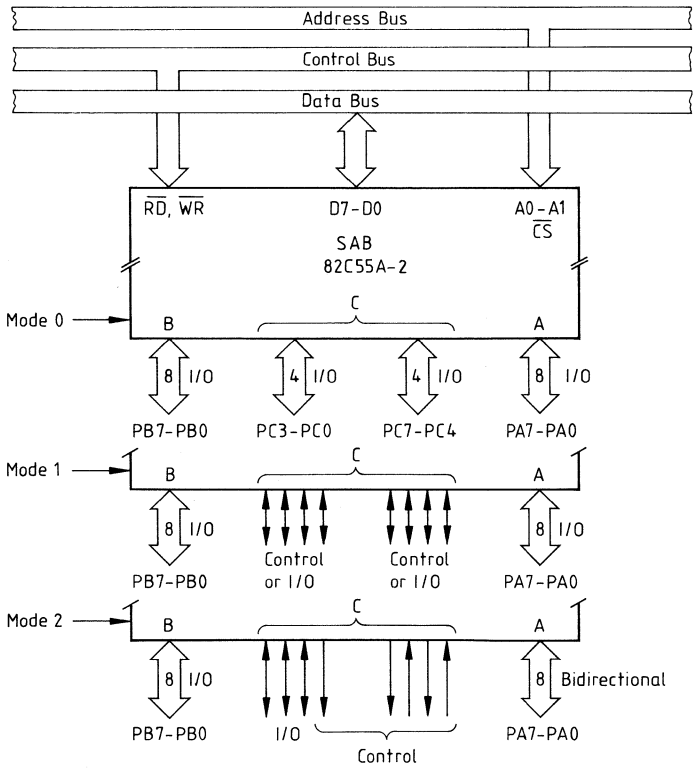
There are three basic modes of operation that can be selected by the system software:

Mode 0 – basic input/output
Mode 1 – strobed input/output
Mode 2 – bidirectional bus

When the reset input goes high all ports will be set to the input mode with all 24 port lines held at a logic "one" level by the internal bus-hold devices (see footnote in figure 3). After the reset is removed the SAB 82C55A-2 can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single SAB 82C55A-2 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for port A and port B can be separately defined, while port C is divided into two portions as required by the port A and port B definitions. All of the output registers, including the status flipflops, will be reset whenever the mode is changed.

Figure 4
Basic Mode Definitions and Bus Interface

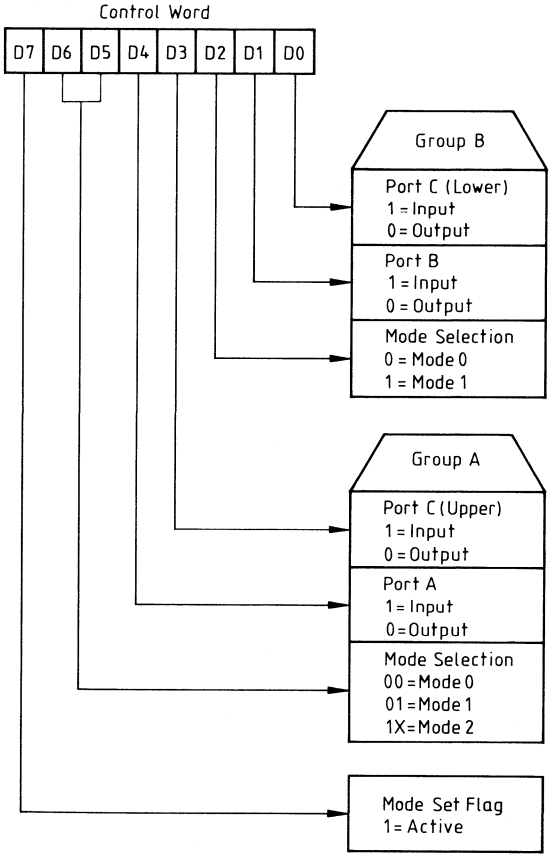


Modes may be combined so that their functional definition can be tailored to almost any I/O structure.

For instance: group B can be programmed in mode 0 to monitor simple switch closings or display computational results, group A could be programmed in mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the SAB 82C55A-2 has taken into account things such as efficient pc board layout, control signal definition versus pc layout, and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Figure 5
Mode Definition Format



Single Bit Set/Reset Feature

Any of the eight bits of port C can be set or reset using a single output instructions. This feature reduces software requirements in control-based applications.

When port C is being used as status/control for port A or B, these bits can be set or reset by using the bit set/reset operation just as if they were data output ports.

Interrupt Control Functions

When the SAB 82C55A-2 is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flipflop, using the bit set/reset function of port C.

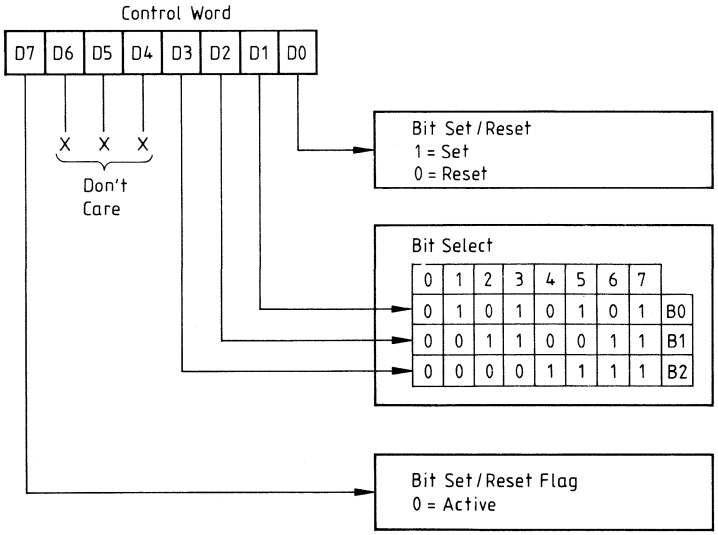
This function permits the programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flipflop definition:

(bit set) – INTE is set – interrupt enable
(bit reset) – INTE is reset – interrupt disable

Note:
All mask flipflops are automatically reset during mode selection and device reset.

Figure 6
Bit Set/Reset Format



Operating Modes

Mode 0 (basic input/output)
This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 basic functional definitions:
- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different I/O configurations are possible in this mode

Figure 7
Mode 0 (basic input)

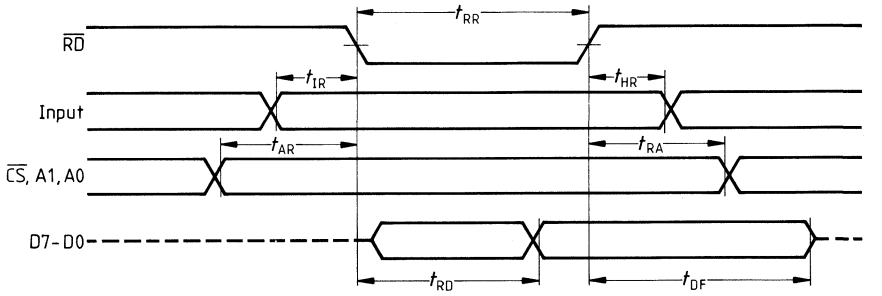
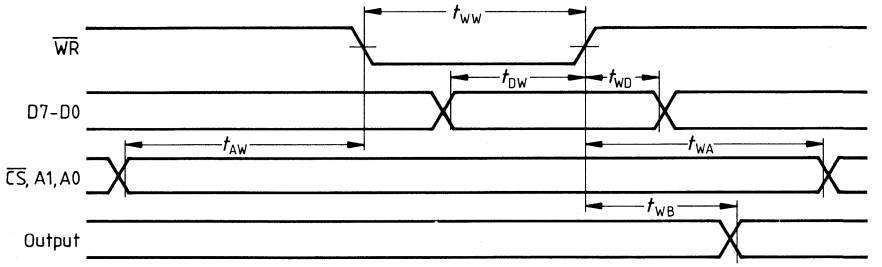


Figure 8
Mode 0 (basic output)



Mode 0 Port Definition

A		B		Group A		No.	Group B	
D4	D3	D1	D0	Port A	Port C (Upper)		Port B	Port C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 1 (strobed input/output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 basic functional definitions:

- Two groups (group A and group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{\text{STB}}$ (strobe input) – A low on this input loads data into the input latch.

IBF (input buffer full flipflop) – A high on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. The IBF is set by the $\overline{\text{STB}}$ input being low and is reset by the rising edge of the $\overline{\text{RD}}$ input.

INTR (interrupt request) – A high on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{\text{STB}} = 1$, IBF = 1, and INTE = 1. It is reset by the falling edge of $\overline{\text{RD}}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A – Controlled by bit set/reset of PC4

INTE B – Controlled by bit set/reset of PC2

Figure 9
Mode 1 Input

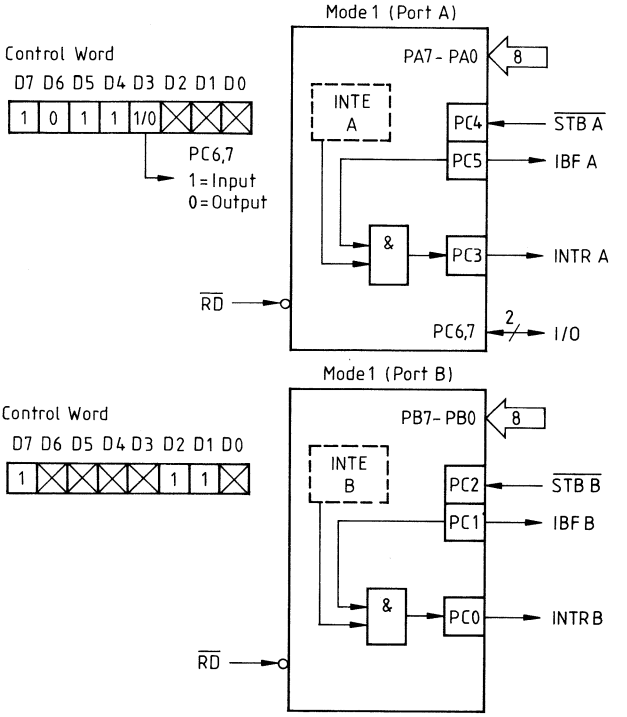
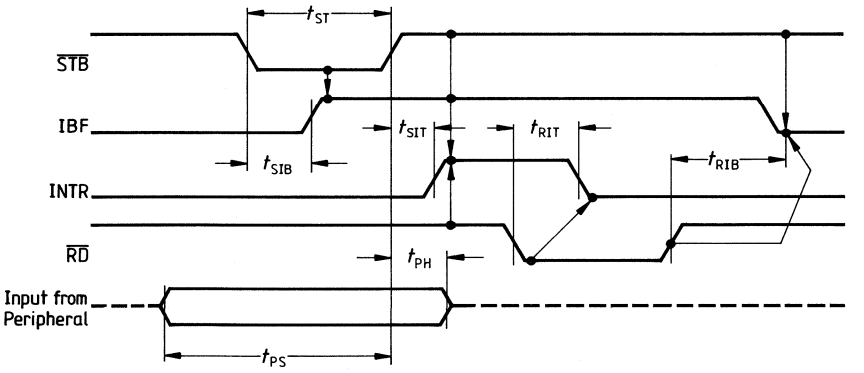


Figure 10
Mode 1 (strobed input)



Output Control Signal Definition

$\overline{OBF}$ ($\overline{output\ buffer\ full\ flipflop}$) – The $\overline{OBF}$ output will go low to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ flipflop will be set by the rising edge of the $\overline{WR}$ input and reset by the $\overline{ACK}$ input being low.

$\overline{ACK}$ ($\overline{acknowledge\ input}$) – A low on this input informs the SAB 82C55A-2 that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (interrupt request) – A high on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ = 1, $\overline{OBF}$ = 1 and INTE = 1. It is reset by the falling edge of $\overline{WR}$.

INTE A – Controlled by bit set/reset of PC6.

INTE B – Controlled by bit set/reset of PC2.

Figure 11
Mode 1 Output

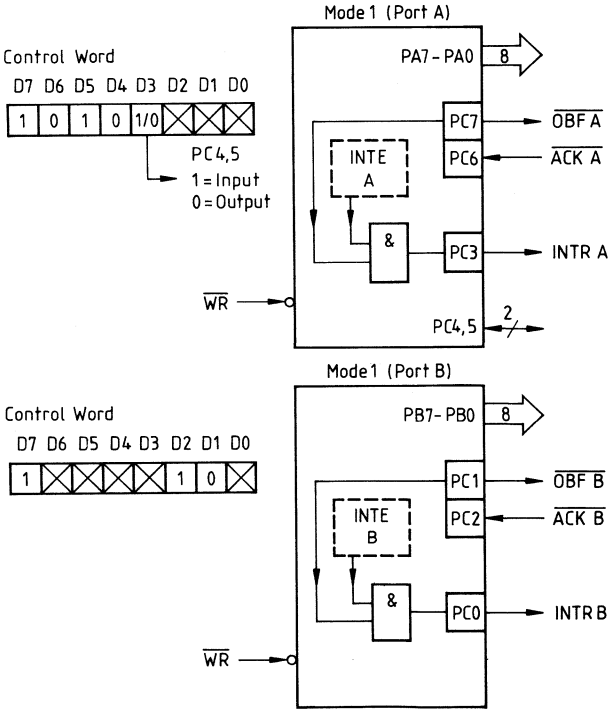
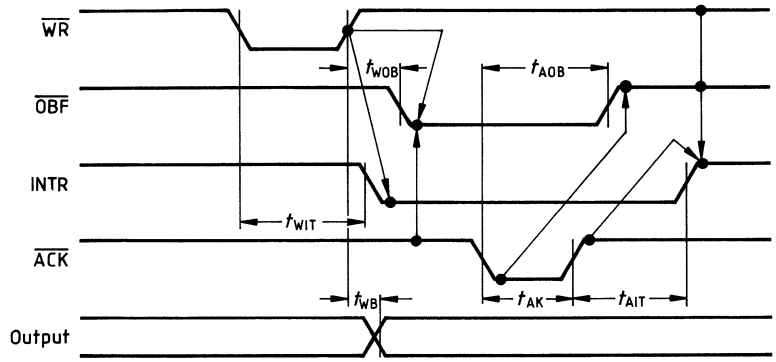


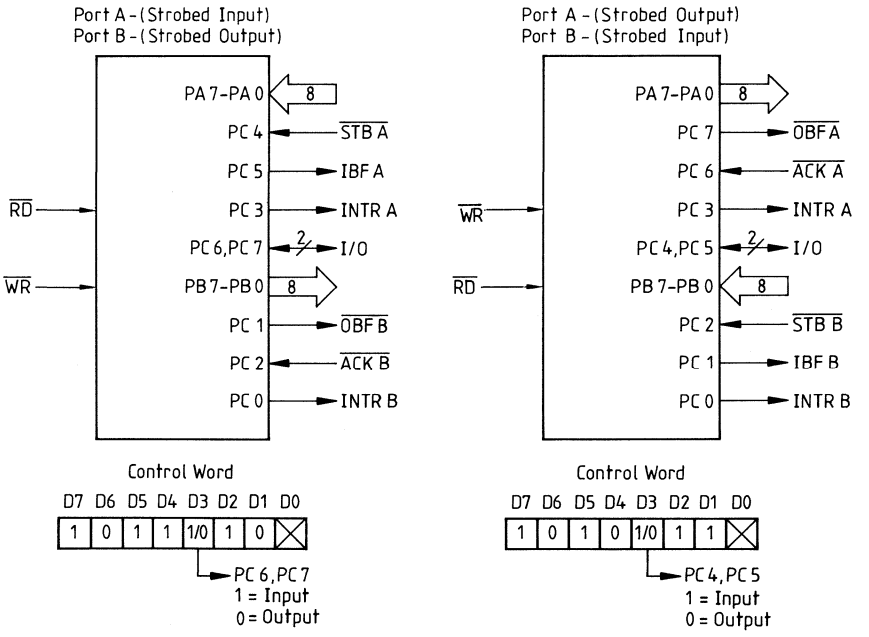
Figure 12
Mode 1 (strobed output)



Combinations of mode 1

Port A and port B can be individually defined as input or output in mode 1 to support a wide variety of strobed I/O applications.

Figure 13
Combinations of Mode 1



Mode 2 (strobed bidirectional bus I/O)
This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a manner similar to mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 basic functional definitions:

- Used in group A only.
- One 8-bit, bidirectional bus port (port A) and a 5-bit control port (port C).
- Both inputs and outputs are latched.
- The 5-bit control port (port C) is used for control and status for the 8-bit, bidirectional bus port (port A).

Bidirectional Bus I/O Control Signal Definition

INTR (interrupt request) – A high on this output can be used to interrupt the CPU for input or output operation.

Output Operations

$\overline{\text{OBF}}$ (output buffer full) – The $\overline{\text{OBF}}$ output will go low to indicate that the CPU has written data out to port A.

$\overline{\text{ACK}}$ (acknowledge) – A low on this input enables the tristate output buffer of port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTE 1 (the INTE flipflop associated with $\overline{\text{OBF}}$) – Controlled by bit set/reset of PC6.

Input Operations

$\overline{\text{STB}}$ (strobe input) – A low on this input loads data into the input latch.

IBF (input buffer full flipflop) – A high on this output indicates that data has been loaded into the input latch.

INTE 2 (the INTE flipflop associated with IBF) – Controlled by set/reset of PC4.

Figure 14
Mode Control Word

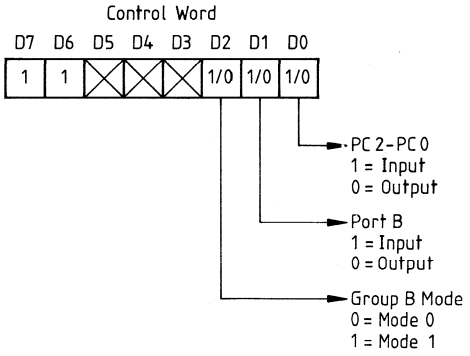


Figure 15
Mode 2

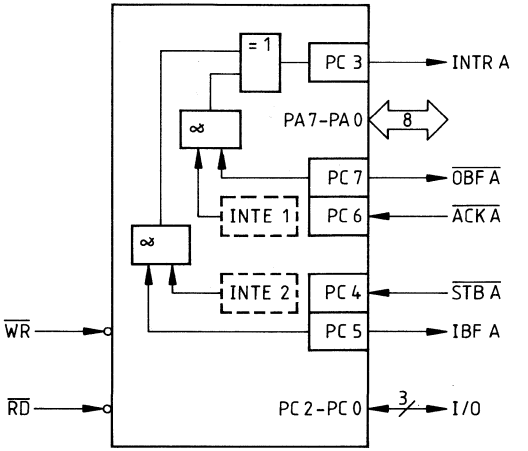
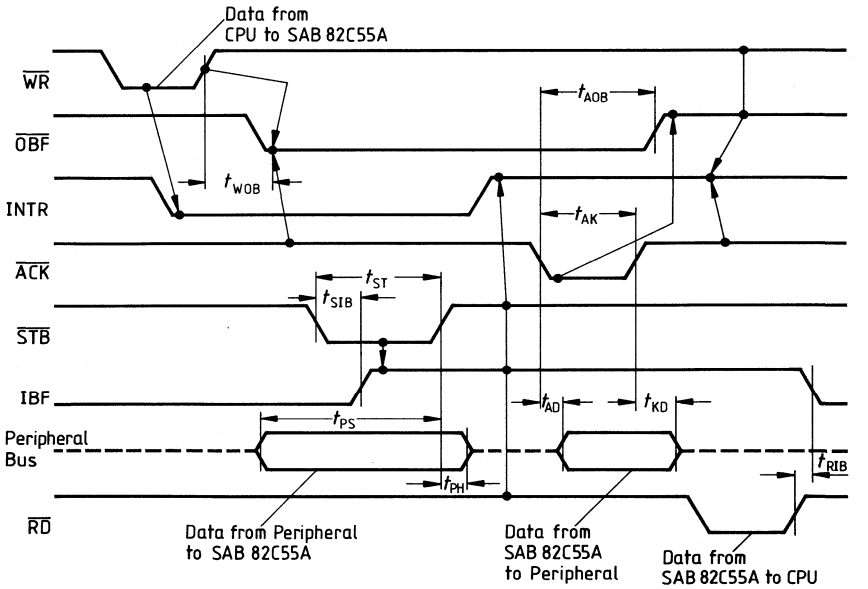
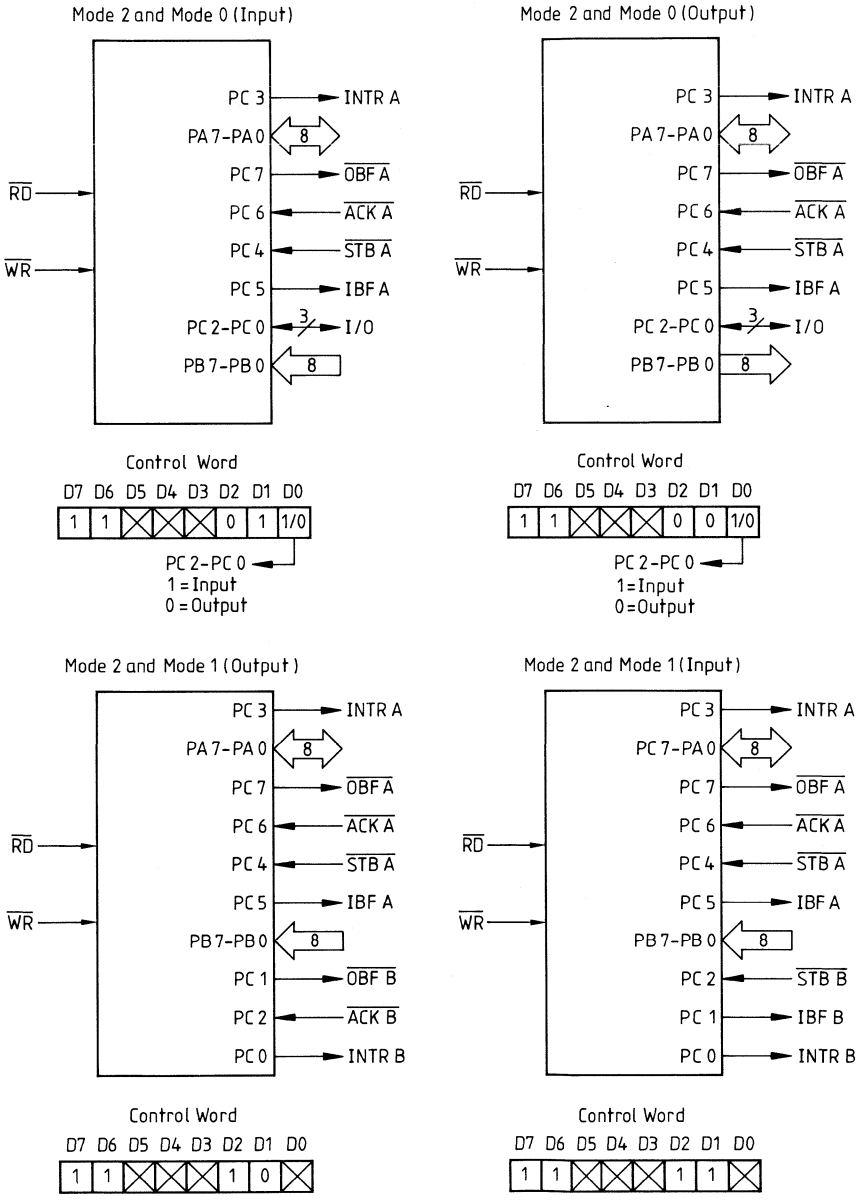


Figure 16
Mode 2 (bidirectional)



Note:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

Figure 17
Mode 1/4 Combinations



Mode Definition Summary

	Mode 0		Mode 1		Mode 2	
	In	Out	In	Out	Group A Only	
PA0	In	Out	In	Out	⟷	
PA1	In	Out	In	Out	⟷	
PA2	In	Out	In	Out	⟷	
PA3	In	Out	In	Out	⟷	
PA4	In	Out	In	Out	⟷	
PA5	In	Out	In	Out	⟷	
PA6	In	Out	In	Out	⟷	
PA7	In	Out	In	Out	⟷	
PB0	In	Out	In	Out	–	Mode 0 or Mode 1 Only
PB1	In	Out	In	Out	–	
PB2	In	Out	In	Out	–	
PB3	In	Out	In	Out	–	
PB4	In	Out	In	Out	–	
PB5	In	Out	In	Out	–	
PB6	In	Out	In	Out	–	
PB7	In	Out	In	Out	–	
PC0	In	Out	INTR B	INTR B	I/O	
PC1	In	Out	IBF B	$\overline{\text{OBF B}}$	I/O	
PC2	In	Out	$\overline{\text{STB B}}$	$\overline{\text{ACK B}}$	I/O	
PC3	In	Out	INTR A	INTR A	INTR A	
PC4	In	Out	$\overline{\text{STB A}}$	I/O	$\overline{\text{STB A}}$	
PC5	In	Out	IBF A	I/O	IBF A	
PC 6	In	Out	I/O	$\overline{\text{ACK A}}$	$\overline{\text{ACK A}}$	
PC7	In	Out	I/O	$\overline{\text{OBF A}}$	$\overline{\text{OBF A}}$	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "set mode" command.

While port C is read, the state of all the port C lines, except the $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ lines, will be placed on the data bus. In place of the $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated in figure 20.

Through a "write port C" command, only the port C pins programmed as outputs in a mode 0 group can be written to. No other pins can be affected by a "write port C" command, nor can the interrupt enable flags be accessed. To write to any port C output programmed as an output in a mode 1 group or to change an interrupt enable flag, the "set/reset port C bit" command must be used.

With a "set/reset port C bit" command, any port C line programmed as an output (including INTR, IBF and $\overline{\text{OBF}}$) can be written to, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ lines, associated with port C are not affected by a "set/reset port C bit" command. Writing to the corresponding port C bit positions of the $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ lines with the "set/reset port C bit" command will affect the group A and group B interrupt anable flags, as illustrated in figure 20.

Current Drive Capability

Any output on port A, B or C can sink or source 2.5 mA. This feature allows the SAB 82C55A-2 to directly drive darlington-type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In mode 0, Port C transfers data to or from the peripheral device. When the SAB 82C55A-2 is programmed to function in modes 1 or 2, port C generates or accepts "handshaking" signals with the peripheral device. Reading the contents of port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from port C. A normal read operation of port C is executed to perform this function.

Figure 18
Mode 1 Status Word Format

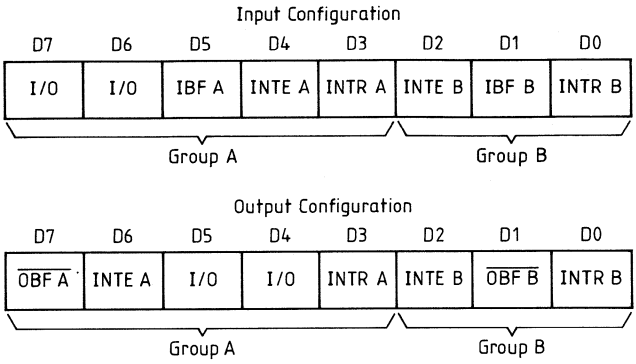


Figure 19
Mode 2 Status Word Format

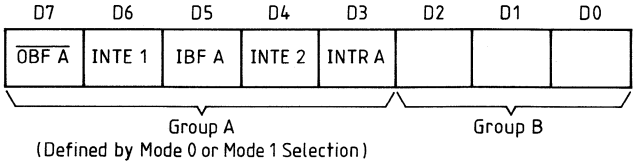


Figure 20
Interrupt Enable Flags in Modes 1 and 2

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (mode)
INTE B	PC2	$\overline{\text{ACK B}}$ (output mode 1) or $\overline{\text{STB B}}$ (input mode 1)
INTE A2	PC4	$\overline{\text{STB A}}$ (input mode 1 or mode 2)
INTE A1	PC6	$\overline{\text{ACK A}}$ (output mode 1 or mode 2)

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Supply voltage	−0.5 to +8.0 V
Operating voltage	4 to 7 V
Voltage on any input	GND −2 V to $+V_{CC}$ +0.5 V
Voltage on any output	GND −0.5 V to V_{CC} +0.5 V
Power dissipation	1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ±10%, GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.0	V_{CC}+0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC}−0.4	–	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input leakage current	–	±1	µA	V_{IN} = V_{CC} to 0 V [1]
I_{OFL}	Output float leakage current	–	±10	µA	V_{IN} = V_{CC} to 0 V [2]
I_{DAR}	Darlington drive current	±2.5	–	mA	Ports A, B, C R_{ext} = 750 Ω V_{ext} = 1.5 V
I_{PHL}	Port hold low leakage current	+50	+300	µA	V_{OUT} = 1.0 V Port A only
I_{PHH}	Port hold high leakage current	−50	−300	µA	V_{OUT} = 3.0 V Ports A, B, C
I_{PHLO}	Port hold low overdrive current	−350	–	µA	V_{OUT} = 0.8 V
I_{PHHO}	Port hold high overdrive current	+350	–	µA	V_{OUT} = 3.0 V
I_{CC}	V_{CC} supply current, average	–	5	mA	[3]
I_{CCSB}	V_{CC} supply current, standby	–	10	µA	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open

Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	

[1]) Pins A1, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, RESET
[2]) Data bus; ports B, C
[3]) I/O write cycle time: 1 µs

AC Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ±10%; GND = 0 V

Bus Parameters

Read Cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AR}	Address stable before $\overline{RD}\downarrow$	0	–	ns	–
t_{RA}	Address hold time after $\overline{RD}\uparrow$	0	–	ns	–
t_{RR}	$\overline{RD}$ pulse width	150	–	ns	–
t_{RD}	Data delay from $\overline{RD}\downarrow$	–	100	ns	[1]
t_{DF}	$\overline{RD}\uparrow$ to data floating	10	40	ns	[2]
t_{RV}	Recovery time between $\overline{RD}/\overline{WR}$	150	–	ns	–

Write Cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AW}	Address stable before $\overline{WR}\downarrow$	0	–	ns	–
t_{WA}	Address hold time after $\overline{WR}\uparrow$	20	–	ns	Ports A and B
		20	–	ns	Port C
t_{WW}	$\overline{WR}$ pulse width	100	–	ns	–
t_{DW}	Data setup time before $\overline{WR}\uparrow$	100	–	ns	–
t_{WD}	Data hold time after $\overline{WR}\uparrow$	30	–	ns	Ports A and B
		30	–	ns	Port C

[1] INTR ↑ may occur as early as $\overline{WR}\downarrow$.

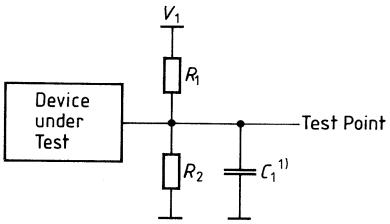
[2] Pulse width of initial reset pulse after power-on must be at least 50 µs. Subsequent reset pulses may be 500 ns minimum.

Other Timings

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{WB}	$\overline{WR}$ = 1 to output	–	350	ns	[1]
t_{IR}	Peripheral data before $\overline{RD}$	0	–	ns	–
t_{HR}	Peripheral data after $\overline{RD}$	0	–	ns	–
t_{AK}	$\overline{ACK}$ pulse width	200	–	ns	–
t_{ST}	$\overline{STB}$ pulse width	100	–	ns	–
t_{PS}	Peripheral data before $\overline{STB}$ high	20	–	ns	–
t_{PH}	Peripheral data after $\overline{STB}$ high	50	–	ns	–
t_{AD}	$\overline{ACK}$ = 0 to output	–	175	ns	[1]
t_{KD}	$\overline{ACK}$ = 1 to output float	20	250	ns	[2]
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0	–	150	ns	[1]
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1	–	150	ns	[1]
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1	–	150	ns	[1]
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0	–	150	ns	[1]
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0	–	200	ns	[1]
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1	–	150	ns	[1]
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1	–	150	ns	[1]
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0	–	200	ns	[1]
t_{RES}	Reset pulse width	500	–	ns	[2]

[1]) INTR ↑ may occur as early as $\overline{WR}$ ↓.
[2]) Pulse width of initial reset pulse after power-on must be at least 50 µs. Subsequent reset pulses may be 500 ns minimum.

AC Test Circuit



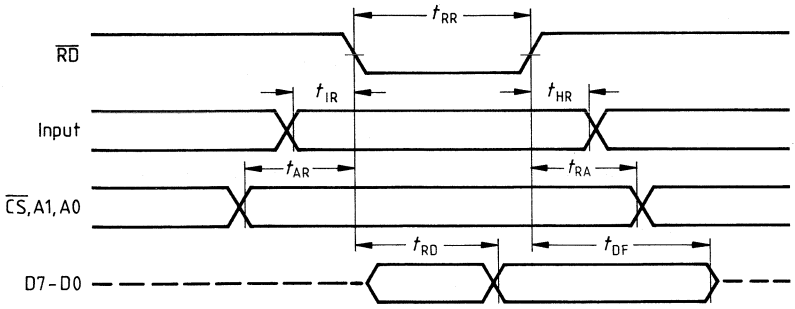
[1]) Includes Stray and Jig Capacitance

Test Condition Definition

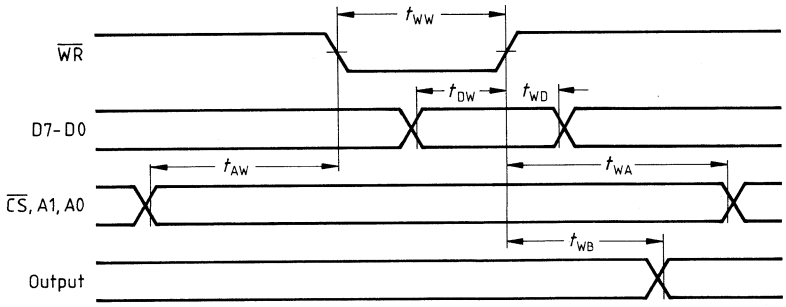
Test Condition	V_1	R_1	R_2	C_1
1	1.7 V	523 Ω	Open	150 pF
2	5.0 V	2 kΩ	1.7 kΩ	50 pF
3	1.5 V	750 Ω	Open	Open

Waveforms

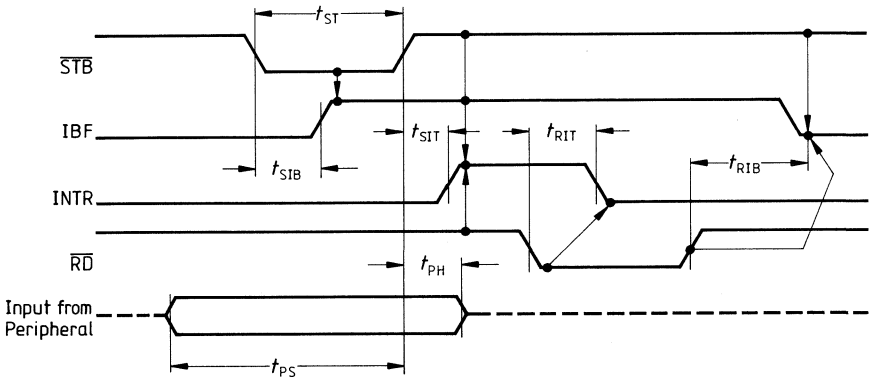
Mode 0 (basic input)



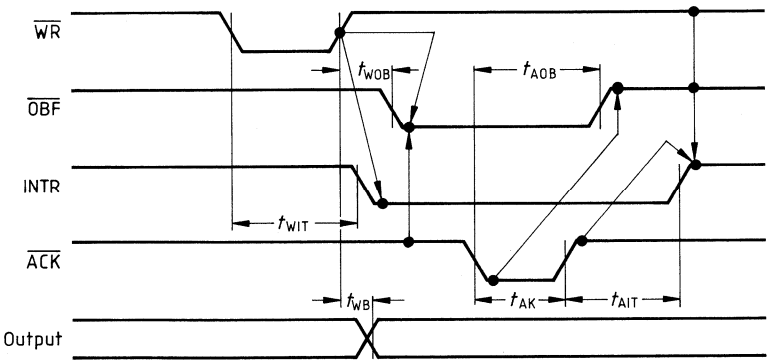
Mode 0 (basic output)



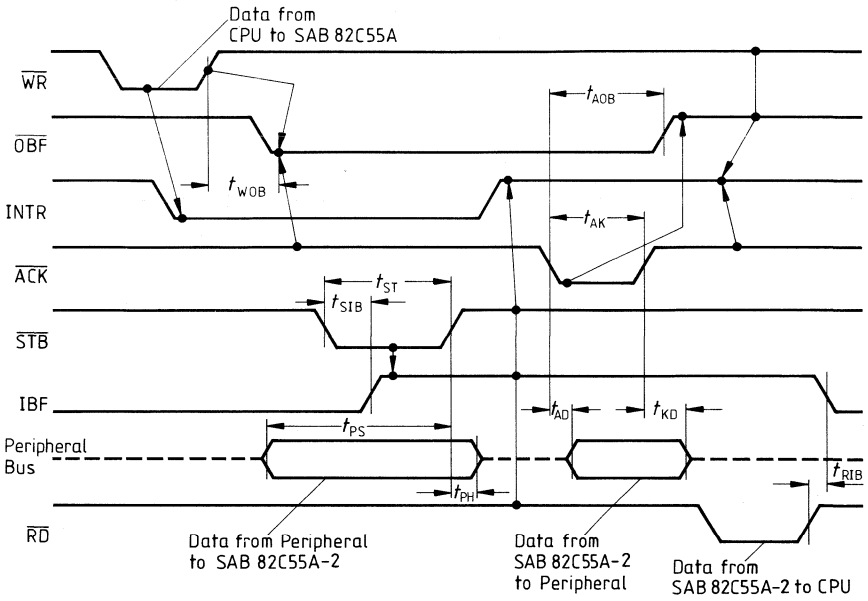
Mode 1 (strobed input)



Mode 1 (strobed output)

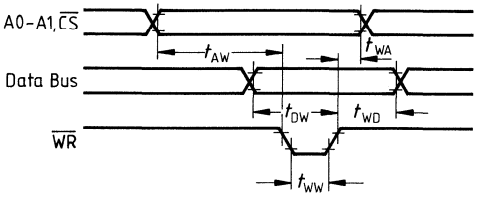


Mode 2 (bidirectional)

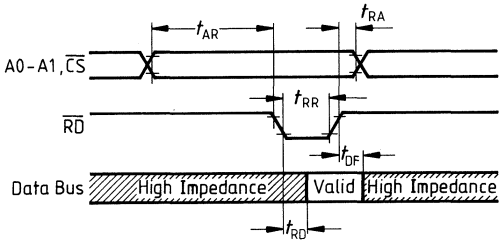


Note:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

Write Timing

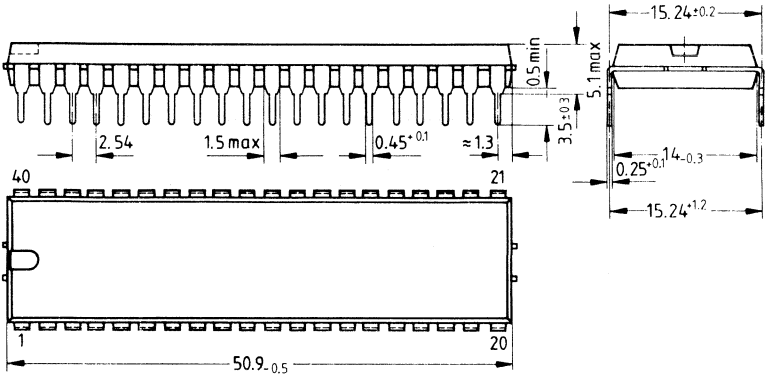


Read Timing



Package Outlines

Plastic Package, P-DIP-40
(dual-in-line package)
20 B 40 DIN 41870 T 10



Dimensions in mm

Ordering Information

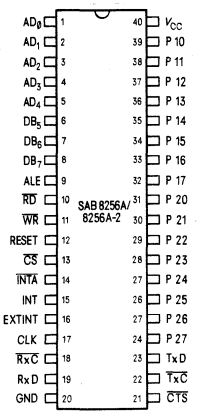
Type	Ordering code	Description
SAB 82C55A-2-P	Q67120-P213	Programmable peripheral interface

Preliminary

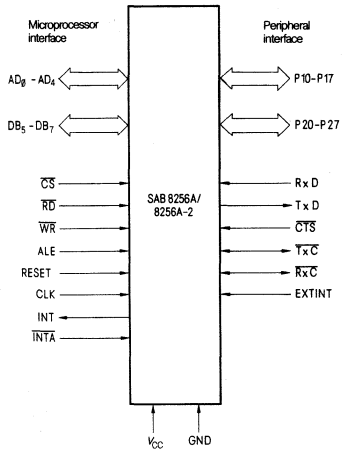
SAB 8256A, SAB 8256A-2 Programmable Multifunction UART (MUART)

- SAB 8256A compatible with processors up to 3 MHz system clock (e. g. SAB 8085A, SAB 8048, SAB 8051).
  SAB 8256A-2 compatible with processors up to 8 MHz system clock (e.g. SAB 8085A-2, SAB 8086 - minimum mode, SAB 80186).
- Full-Duplex asynchronous serial interface with programmable 5–8 data bits, 0.75–2 stop bits, parity generation and checking.
- Internal baud rate generator programmable for 50–19200 Baud; 0–1 Megabaud possible with external baud rate clock.
- Interrupt Controller with 8 priority levels; each level independently maskable, programmable for normal and fully nested operation with SAB 8085 and SAB 8086 processor families.
- Five programmable 8-bit counter/timers, internal or external clock, four are cascadable to two 16-bit counter/timers.
- Two 8-bit I/O ports, bit programmable for input/output, hand-shake mode supported.

Pin Configuration



Logic Symbol



SAB 8256A integrates four of the most used peripheral functions in a microcomputer system into a 40 pin package: serial interface, parallel interface, timer/counter and interrupt controller. It is primarily suited for system like SAB 8048, SAB 8051, SAB 8085, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 which have a multiplexed bus. With some additional circuitry, it can also be used with other processors. All the functions of SAB 8256A are programmable by software, leading to a great flexibility in system design.

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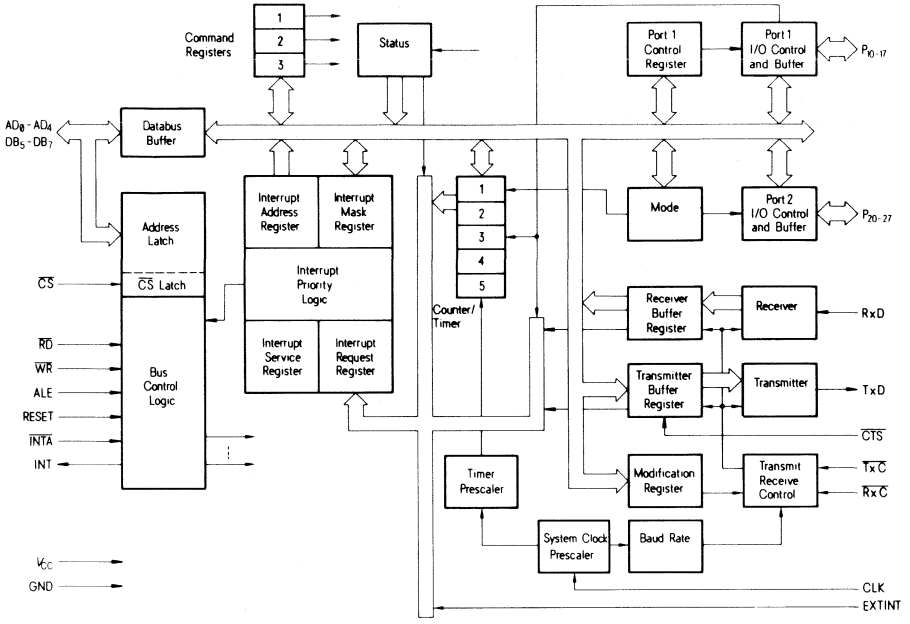
Pin Description and Functions

Symbol	Pin No.	Input (I) Output (O)	Function
AD$\emptyset$–AD4, DB5–DB7	1–8	I/O	**Interface to Multiplexed Bus** Bidirectional lines to 8 data bits and 5 least significant address bits which are latched internally on the falling edge of ALE.
ALE	9	I	**Adress Latch Enable** The five least significant address bits and $\overline{CS}$ are latched on the falling edge of ALE into an internal register.
$\overline{RD}$	10	I	**Read Control** The microprocessor reads data from the chip when this signal is low.
$\overline{WR}$	11	I	**Write Control** The microprocessor writes data into the chip with a low on this pin.
RESET	12	I	**Reset** A high on this pin forces the chip to its initial state. The chip remains in this state till control information is written into the chip.
$\overline{CS}$	13	I	**Chip Select** A low on this pin during ALE enables the bus interface of the chip. Neither read nor write operations are possible without this enable. The signal has no effect on the internal operation of the chip.
$\overline{INTA}$	14	I	**Interrupt Acknowledge** The microprocessor informs the chip a low on this pin that an interrupt request is being serviced, if this functions has been enabled.
INT	15	O	**Interrupt Request** The chip demands interrupt service from the microprocessor with a high on this output.
EXTINT	16	I	**External Interrupt** An external source can request interrupt service through this input. The source can be either a peripheral or another SAB 8256A with its INT pin as the signal source. The input is level sensitive (high). The request must be held high until the processor acknowledges it.
CLK	17	I	**System Clock** Clock on this input is the reference clock for various function like timers, baud rate generator etc.

Symbol	Pin No.	Input (I) Output (O)	Function
$\overline{R \times C}$	18	I/O	**Receiver Clock** If this pin is programmed as an output, it provides a low-to-high transition at the sampling point of each received data bit (excluding the framing bits). When programmed as an input, an externally generated receiver clock must be connected to this pin. At DC, its frequency can range up to 1.024 MHz matching the receiver baud rate. The internal baud rate generator is disabled if this pin is used as input.
R×D	19	I	**Receiver Data** Input for serial data, which is converted to parallel format while discarding the framing bits and then is made available for the processor.
$\overline{CTS}$	21	I	**Clear to Send** This input enables the serial transmitter. If 1, 1.5 or 2 stop bits are selected, $\overline{CTS}$ is level sensitive. As long as $\overline{CTS}$ is low, any character loaded into the transmitter buffer register will be transmitted serially. For continuous transmission, this input must be tied to low. A single negative going pulse causes the transmission of a single character previously loaded into the transmitter buffer register. If the transmitter buffer is empty, this pulse will be ignored. If this pulse occurs during the transmission of a character upto the time where 0.5 of the first (or the only) stop bit is sent out, it will be ignored. If it occurs afterwards, but before the end of the stop bits the next character will be transmitted immediatly following the current one. If $\overline{CTS}$ is still high when the transmitter register is sending the last stop bit, the transmitter will enter its idle state until the next high-to-low transition on $\overline{CTS}$ occurs. If 0.75 stop bits is chosen, $\overline{CTS}$ input is edge sensitive. A negative edge on $\overline{CTS}$ results in the immediate transmission of the next character. The length of the stop bits is determined by the time interval between the beginning of the first stop bit and the next negative edge on $\overline{CTS}$. A high-to-low transition has no effect if the transmitter buffer is empty or if the time interval between the beginning of the stop bit and next negative edge is less than 0.75 bit. A high or a low level or a low-to-high transition has no effect on the transmitter for the 0.75 stop bit mode.
$\overline{T \times C}$	22	I/O	**Transmitter Clock** The function of this pin can be programmed in 3 configurations. As an output it delivers the transmitter clock corresponding to the baud rate. If programmed as an input, an external clock of 32 or 64 times the baud rate that is common to transmitter and receiver, or a 1× clock matching the baud rate which is used for the transmitter only, can be tied to this pin. The maximum frequency is 1.024 MHz. Thus, baud rates ranging from 0 to 16 Kbaud (64×) or from 0 to 32 Kbaud (32×) or from 0 to 1.024 Mbaud (1×) are possible. The internal baud rate generator is disabled if $\overline{T \times C}$ is selected as input.

Symbol	Pin No.	Input (I) Output (O)	Function
T×D	23	O	**Transmitter Data** Serial data output. The parallel data received from the processor and the framing bits added by the SAB 8256A are sent out serially over this output when the transmitter is enabled by the $\overline{CTS}$ signal.
P27–P20	24–31	I/O	**Parallel I/O Port 2** The eight general purpose I/O pins of parallel port 2 can be configured in sets of four pins (nibbles) as inputs or outputs or 8 bit I/O with handshake (control-signals at port 1). In the nibble mode the output signals are latched whereas the input signals are not. In the handshake mode both inputs and outputs are latched.
P17–P10	32–39	I/O	**Parallel I/O Port 1** Each one of these 8 pins can be programmed as input or output. Alternatively these pins can serve as control pins which extends considerably the functional spectrum of the chip. The pins are assigned special functions implicitly by programming. All outputs are latched whereas inputs are not.
V_{CC}	40	–	**Power Supply** (+5 V)
GND	20	–	**Ground** (0 V)

Block Diagram



Functional Description

Bus Interface

The bus interface unit, consisting of bus drivers, address latches and bus control logic, interfaces the SAB 8256A to the data, address and control busses of a microcomputer system. The chip is selected by the $\overline{CS}$ signal, which is latched into the chip along with address lines AD0–AD4 by the ALE signal. $\overline{WR}$ and $\overline{RD}$ signals are used to write data into and read data from SAB 8256A.
Signals INT und $\overline{INTA}$ are used to handle interrupt protocol with the processor.
RESET signal resets the chip to its initial state.

Counter/Timer

Five programmable counter/timers can be used in several modes. Each can be used as an 8-bit timer while two can alternatively serve as counters. Counter/timer 2 and timer 4 as well as 3 counter/timer and timer 5 can be cascaded to 16-bit counter/timers. All counter/timers function as binary down-counters with a programmable initial value and generate an interrupt request on their 1 to 0 transition. An internal register is provided for the initial count of timer 5 and with an external trigger pulse it is possible to reload the initial value into timer 5 (also for cascaded counter/timer 3 and timer 5).
A common clock source with a frequency of either 1 KHz or 16 KHz is available for the timers. In addition, for counters 2, 3 and the cascaded counters, an external clock source can be provided through two pins of part 1.

Asynchronous Serial Interface

For double buffered full-duplex operations both transmitter and receiver have two registers. The received data (5 to 8 data bits, programmable) is assembled to parallel format in the receiver register, the framing bits (Start, Stop, and Parity) are stripped off and stored into the receiver buffer register. The data to be transmitted is first loaded into the transmitter buffer register and then sent out through the transmitter register.
Controlling the $\overline{CTS}$ signal, single characters on character strings can be transmitted. Baud rate clock (50 to 19,200 Baud) is generated on the chip which is common to both the receiver and the transmitter. It is also possible to provide an external baud rate clock (common or separate for receiver and transmitter) to provide baud rates from 0 to 1.024 Mbaud.

Parallel Interface

The parallel interface consists of two 8-bit ports programmable as inputs or outputs. Each pin of port 1 can be programmed separately as an input or an output. They can also be used as control pins. Ports 2 can be programmed as input our output in two 4-bit groups. Port 2 can also be used as an 8-bit input or output port with handshake signals.

Assignment of Control Signals to Port 1

Pins Port 1	P17	P16	P15	P14	P13	P12	P11	P10
Control Function	External interrupt input	Break-In detect input	Trigger input for timer 5 (cascaded counter/timer 3+5)	Output of the clock of the internal baudrate-generator	Clock input for counter 3	Clock input for counter 2	Handshake Control Signals for Port 2	

Interrupt Controller

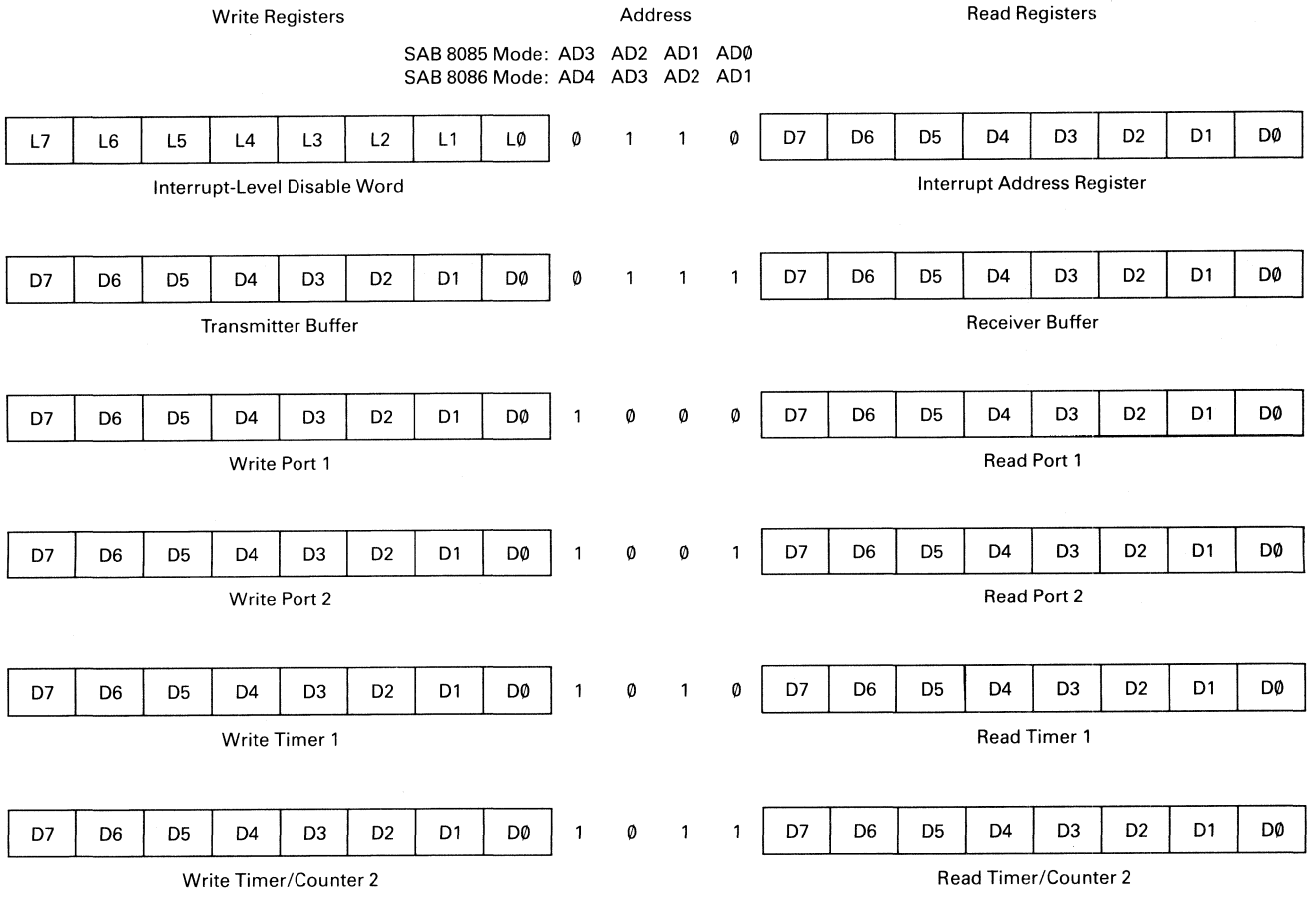
The interrupt controller manages 12 interrupt sources (10 internal and 2 external) on 8 priority levels. Normal (every interrupt request immediately recognized) and "fully nested" (recognition based on priority) modes are supported.
The interrupt controller supports various methods of connecting SAB 8256A to the processor. Firstly, the true interrupt mode (using INT and $\overline{\text{INTA}}$ signals for interrupt protocol), secondly, a combination of polling and interrupt (using INT and interrupt address registers). The interrupt protocols of SAB 8048, SAB 8085A, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 are directly supported.

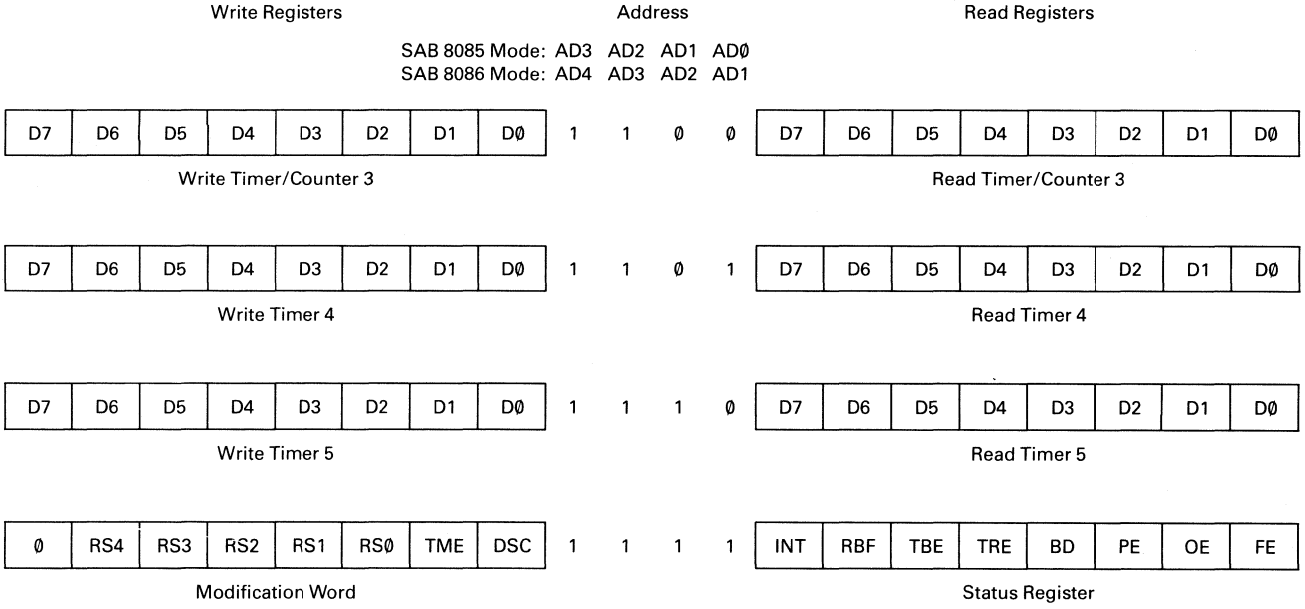
Programming the SAB 8256A

The functional characteristics of SAB 8256A can be programmed by writing appropriate control information into it. It is specially designed for ease of programming. It is hence possible to alter individual bits in certain registers like e.g. the Interrupt Mask Register and Command Register 3. All functions of SAB 8256A can be easily used because each unit (e.g. counter/timer, serial interface) has specially assigned registers which can be directly read or written.

Register Select

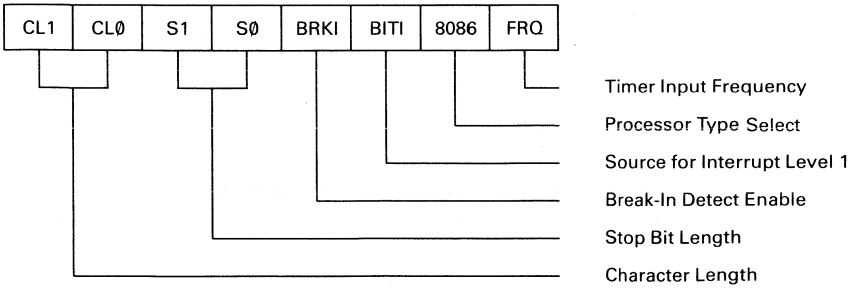
Write Registers								Address				Read Registers							
								SAB 8085 Mode: AD3	AD2	AD1	ADØ								
								SAB 8086 Mode: AD4	AD3	AD2	AD1								
CL1	CLØ	S1	SØ	BRKI	BITI	8086	FRQ	Ø	Ø	Ø	Ø	CL1	CLØ	S1	SØ	BRKI	BITI	8086	FRQ
Command Word 1												Command Register 1							
PEN	EP	C1	CØ	B3	B2	B1	BØ	Ø	Ø	Ø	1	PEN	EP	C1	CØ	B3	B2	B1	BØ
Command Word 2												Command Register 2							
SET	R×E	IAE	NIE	END	SBRK	TBRK	SRES	Ø	Ø	1	Ø	Ø	R×E	IAE	NIE	Ø	SBRK	TBRK	Ø
Command Word 3												Command Register 3							
T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2CØ	Ø	Ø	1	1	T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2CØ
Mode Word												Mode Register							
P17	P16	P15	P14	P13	P12	P11	P1Ø	Ø	1	Ø	Ø	P17	P16	P15	P14	P13	P12	P11	P1Ø
Port 1 Control Word												Port 1 Control Register							
L7	L6	L5	L4	L3	L2	L1	LØ	Ø	1	Ø	1	L7	L6	L5	L4	L3	L2	L1	LØ
Interrupt-Level Enable Word												Interrupt Mask Register							


Write Registers
Address
Read Registers
SAB 8085 Mode: AD3 AD2 AD1 AD0
SAB 8086 Mode: AD4 AD3 AD2 AD1
L7 L6 L5 L4 L3 L2 L1 L0
0 1 1 0
D7 D6 D5 D4 D3 D2 D1 D0
Interrupt-Level Disable Word
Interrupt Address Register
D7 D6 D5 D4 D3 D2 D1 D0
0 1 1 1
D7 D6 D5 D4 D3 D2 D1 D0
Transmitter Buffer
Receiver Buffer
D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0
D7 D6 D5 D4 D3 D2 D1 D0
Write Port 1
Read Port 1
D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 1
D7 D6 D5 D4 D3 D2 D1 D0
Write Port 2
Read Port 2
D7 D6 D5 D4 D3 D2 D1 D0
1 0 1 0
D7 D6 D5 D4 D3 D2 D1 D0
Write Timer 1
Read Timer 1
D7 D6 D5 D4 D3 D2 D1 D0
1 0 1 1
D7 D6 D5 D4 D3 D2 D1 D0
Write Timer/Counter 2
Read Timer/Counter 2

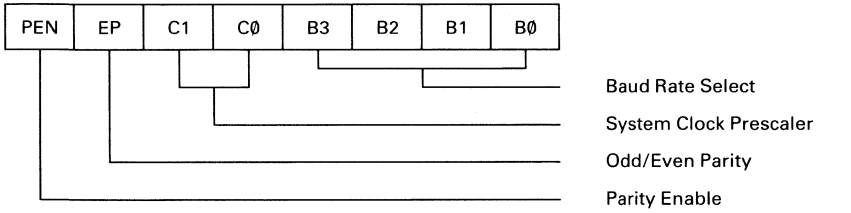

Write Registers
Address
Read Registers
SAB 8085 Mode: AD3 AD2 AD1 AD0
SAB 8086 Mode: AD4 AD3 AD2 AD1
D7 D6 D5 D4 D3 D2 D1 D0
1 1 0 0
Write Timer/Counter 3
Read Timer/Counter 3
1 1 0 1
Write Timer 4
Read Timer 4
1 1 1 0
Write Timer 5
Read Timer 5
0 RS4 RS3 RS2 RS1 RS0 TME DSC
1 1 1 1
Modification Word
INT RBF TBE TRE BD PE OE FE
Status Register

Programming

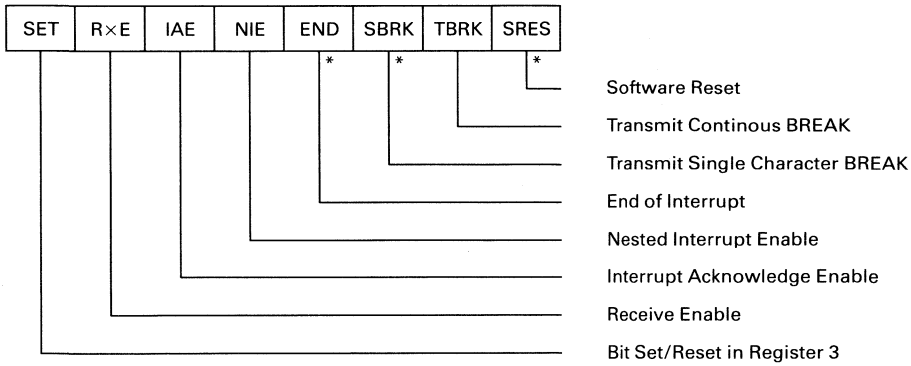
Command Word 1



Command Word 2

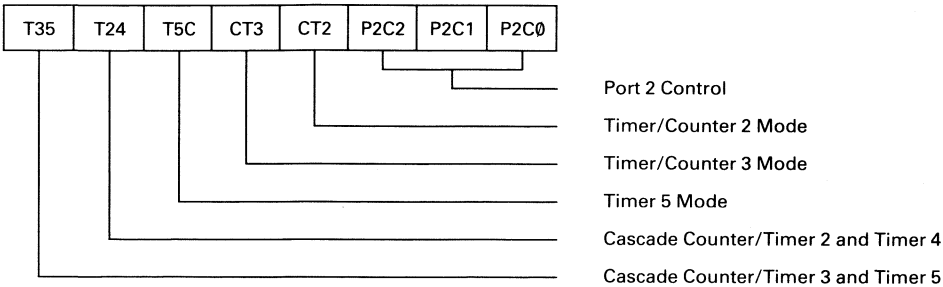


Command Word 3

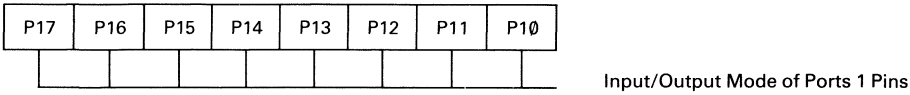


*) These bits can only be set, they are reset at the end of the operation.

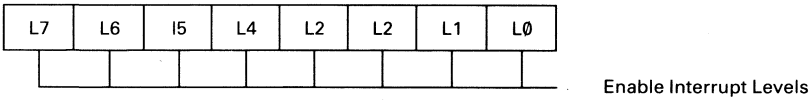
Mode Word



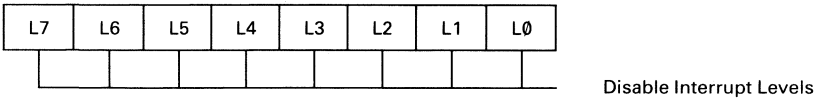
Port 1 Control World



Interrupt-Level Enable Word

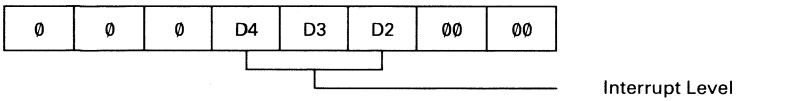


Interrupt-Level Disable Word



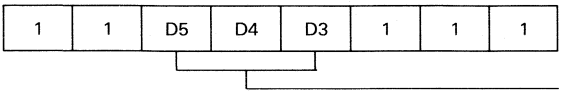
Determination of Interrupt Level

Reading the Interrupt Address Register

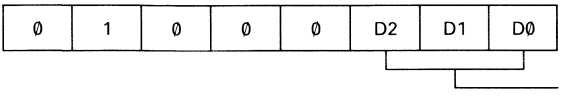


Response to $\overline{INTA}$

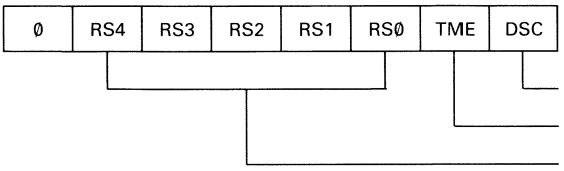
SAB 8085-Mode (RST-instruction in response to $\overline{INTA}$)



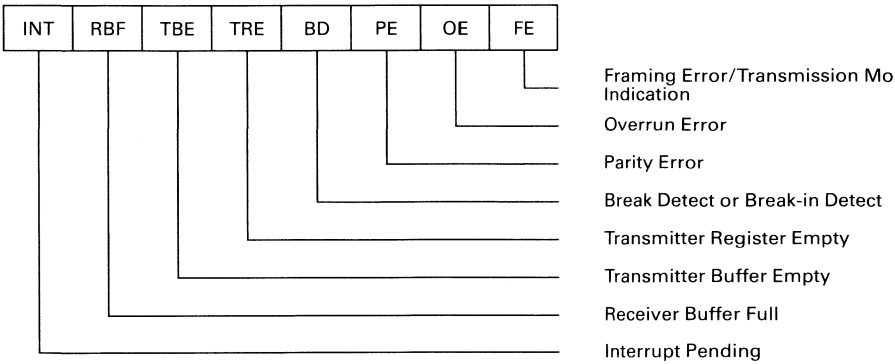
SAB 8086-Mode (Interrupt Vector in response to second $\overline{INTA}$)



Modification Word



Status Register



Absolute Maximum Ratings [1]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin With Respect to Ground	−0.5 to +7 V
Power Dissipation	1 W

D.C. Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V
(if not otherwise specified)

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{IL}	Input Leakage	–	±10	µA	V_{IN} = 0 V to V_{CC}
I_{LO}	Output Leakage Current				V_{OUT} = 0 V to V_{CC}
I_{CC}	V_{CC} Supply Current		190	mA	–

Capacitance [2]

Symbol	Parameter	Limit Value (Max.)	Unit	Test Condition
C_{IN}	Input Capacitance	10	pF	f_C = 1 MHz Unmeasured pins returned to GND
$C_{I/O}$	I/O Capacitance	20		

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ± 5%; V_{SS} = 0V

Test Conditions

Capacitive load C_L = 150 pF

The timings are with respect to the following levels:

H-level: 2.0V
L-level: 0.8V
Rise and fall times: 20 ns

The timings are valid for an internal clock of 1.024 MHz.

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8256A		SAB 8256A-2			
		Min.	Max.	Min.	Max.		
t AC	$\overline{STB}\downarrow$ to $\overline{IBF}\downarrow$	–	300	–	300	ns	–
t ACK	$\overline{ACK}$ Pulse Width	t ADP	–	t ADP	–	–	
t AD	Address Stable to Data Valid	–	400	–	230	ns	
t ADP	$\overline{ACK}\downarrow$ to $\overline{OBF}\uparrow$		300		300		
t AED	$\overline{OBF}\downarrow$ to $\overline{ACK}\downarrow$	0	–	0	–		
t AI	$\overline{ACK}\uparrow$ to INT $\uparrow$	–	1.5 t CY	–	1.5 t CY	–	
t AL	Address Stable to ALE $\downarrow$	50	–	30	–	ns	
t CC	$\overline{RD}$ and $\overline{WR}$ Pulse widths	300		200			
t CL	$\overline{RD}\uparrow$ or $\overline{WR}\uparrow$ to Next ALE $\uparrow$	50		25			
t CPI	Counter input Cycle Time (P12, P13,)	2.2		2.2		µs	
t CSL	$\overline{CS}$ Stable to ALE $\downarrow$	60		10		ns	
t CTS	$\overline{CTS}$ Pulse Width for Single Character Transmission	[1]		[1]		–	
t CY	System Clock Period	300		195		ns	–
t DEI	$\overline{STB}\uparrow$ to INT $\uparrow$	–	1.5 t CY	–	1.5 t CY	–	
t DEX	EXTINT $\uparrow$ to INT $\uparrow$		200		200	ns	
t DH	$\overline{STB}\uparrow$ to P2 Data Stable	10	–	10	–		
t DPI	Interrupt Request on P17 to INT $\uparrow$	–	1.5 t CY	–	1.5 t CY	–	
t DSI	P2 Data Stable before $\overline{STB}\downarrow$	10	–	10	–	ns	
t DTX	$\overline{T\times C}\downarrow$ to T×D Data Valid	–	300	–	300		
t DW	Data Valid before $\overline{WR}\uparrow$	250	–	150	–		
t HEA	EXTINT $\downarrow$ after $\overline{INTA}\uparrow$ or $\overline{RD}\uparrow$	30		30			
t HIA	INT $\downarrow$ after $\overline{INTA}\uparrow$ or $\overline{RD}\uparrow$	–	300	–	300		
t LA	$\overline{CS}$ and Address valid after ALE $\downarrow$	50	–	20	–		
t LC	ALE $\downarrow$ to $\overline{RD}\downarrow$ or $\overline{WR}\downarrow$	60		20			
t LL	ALE Pulse width	100		50			

Notes see next page.

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8256A		SAB 8256A-2			
		Min.	Max.	Min.	Max.		
t PI	Pulse Width of Interrupt Request on P17	1.1	–	1.1	–	µs	–
t PP	Counter 5 Load (P15↓) before Next Clock Pulse on P13 ↑			1.1			
t PR	P1, P2 Data Stable before $\overline{RD}$ ↓	300		300		ns	
t RD	Data Valid after $\overline{RD}$ ↓	–	200	–	150		
t RDE	$\overline{RD}$ ↓ to Data Drivers Active	10	100	10	50		
t RDF	Data Bus Float After $\overline{RD}$ ↑						
t RES	RESET Pulse Width	300	–	300	–		
t RI	$\overline{RD}$ ↑ to $\overline{IBF}$ ↑	–	300	–	300		
t RP	P1, P2 Data Hold after $\overline{RD}$ ↑	50	–	50	–		
t RRD	Data Bit Start to $\overline{R \times C}$ ↓	300	[2]	150	[2]		[3]
t RV	$\overline{RD}$ ↑ or $\overline{WR}$ ↑ to Next $\overline{RD}$ ↓ or $\overline{WR}$ ↓						$\overline{CS}$=Low
t SCY	Serial Clock Period (32×, 64×)	975		975			–
t SPD	Serial Clock High (32×, 64×)	350		350			
t SPW	Serial Clock Low (32×, 64×)						
t STB	Strobe Pulse Width	*t* AC	–	*t* AC	–	–	
t TCY	Serial Clock Period (1×)	975		975		ns	
t TPD	Serial Clock High (1×)	350		350			
t TIH	Load Pulse for Counter 5 (P15)-High	1.1		1.1		µs	
t TIL	Load Pulse for Counter 5 (P15)-Low						
t TPI	Counter Input ↑ (P12, P13) to INT ↑ at Terminal Count	–	2.5	–	2.5		
t TPW	Serial Clock Low (1)	350		350		ns	–
t TRV	Time between 2 readcycles onto the same counter/timer	1.1	–	1.1	–	µs	
t WD	Data Hold after $\overline{WR}$ ↑	40		30		ns	
t WP	P1, P2 Data Valid after $\overline{WR}$ ↑	–	300	–	300		
t WPH	Count Clock (P12, P13) High	1.1	–	1.1	–	µs	
t WPL	Count Clock (P12, P13) Low						
t WPO	$\overline{OBF}$ ↑ after $\overline{WR}$ ↓	–	300	–	300	ns	
t f	Clock Fall Time		30		30		
t ΦH	Clock High	105	–	65	–		
t ΦL	Clock Low						
t r	Clock Rise Time	–	30	–	30		

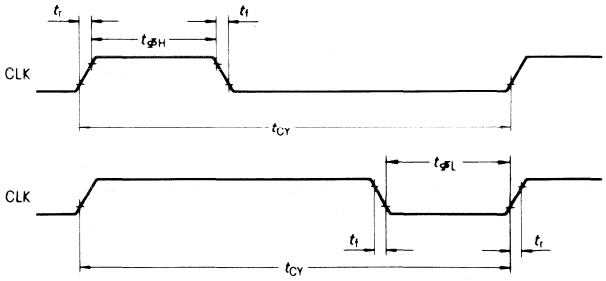
[1] 1/32 bit length with transmitter clock with a baud rate factor of 32 or 64
100 ns when baud rate factor = 1

[2] 300 ns + (1/32 bit length)

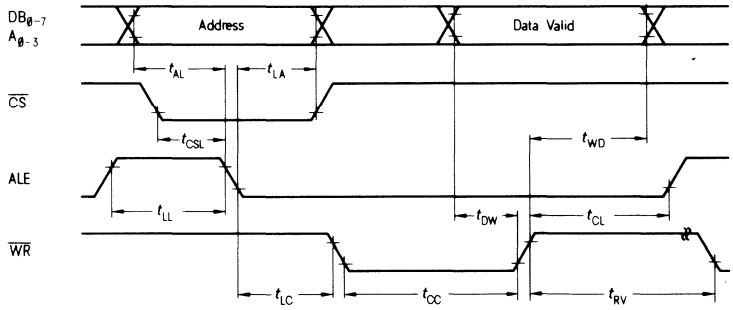
[3] Sampling time at bit center

Waveforms

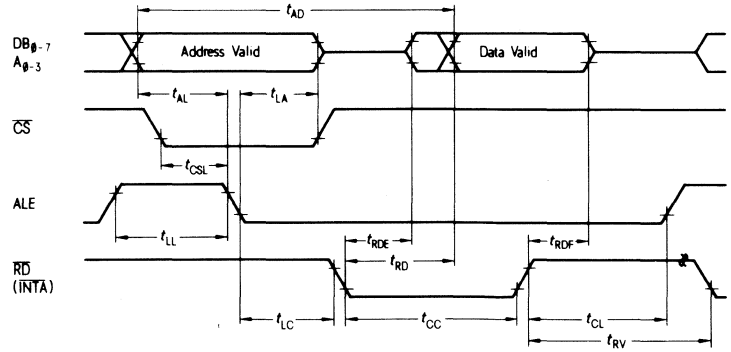
System Clock



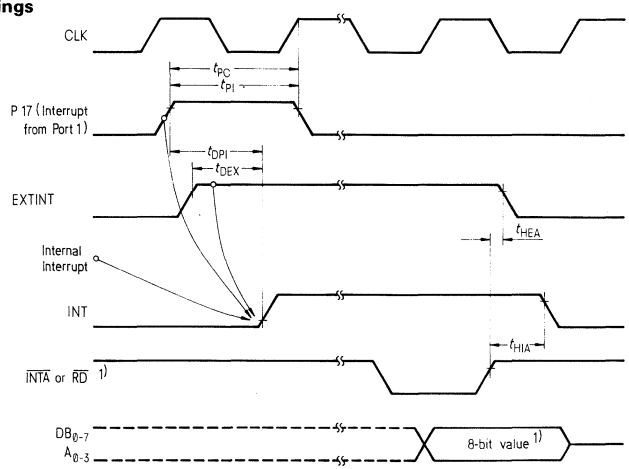
Write Cycle (Processor → SAB 8256A)



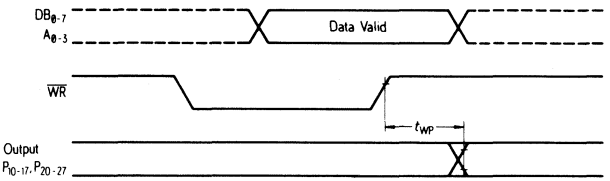
Read Cycle (SAB 8256A → Processor)



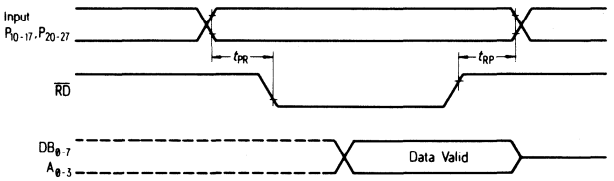
Interrupt Timings



Basic Output from Port 1 and Port 2

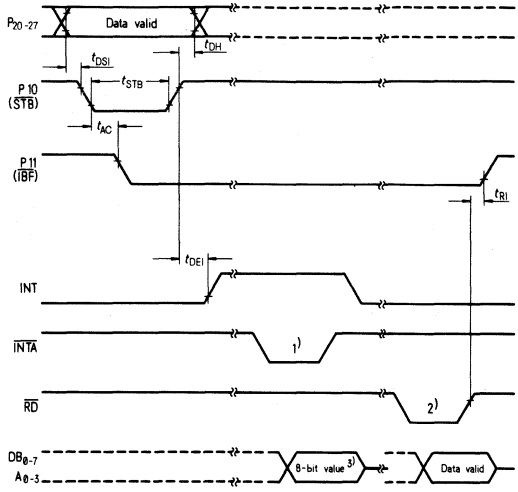


Basic Input from Port 1 and Port 2

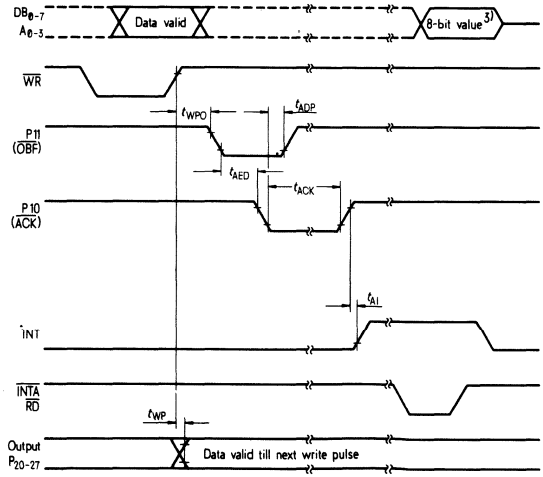


1) If INTA is enabled, RSTn instruction is output on INTA (SAB 8085 mode) or interrupt vector is output on second INTA (SAB 8086 mode) otherwise, interrupt address is output on a read address register operation.

Input from Port 2 in Hand-shake mode
(Control signals from Port 1)

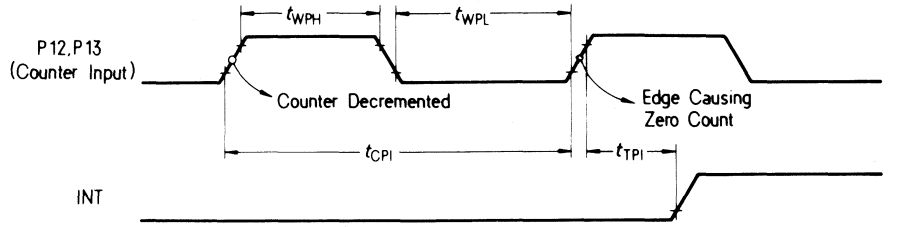


Output from Port 2 in Hand-shake mode
(Control signals from Port 1)

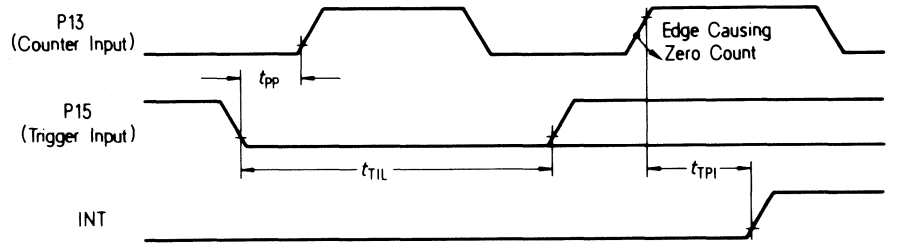


1) Instead of $\overline{INTA}$, $\overline{RD}$ can serve as interrupt acknowledge (reading the interrupt address register).
2) Read from channel 2.
3) If $\overline{INTA}$ is enabled, RSTn instruction is output on $\overline{INTA}$ (SAB 8085 mode) or interrupt vector is output on second $\overline{INTA}$ (8086 mode) otherwise, interrupt address is output on a read address register operation.

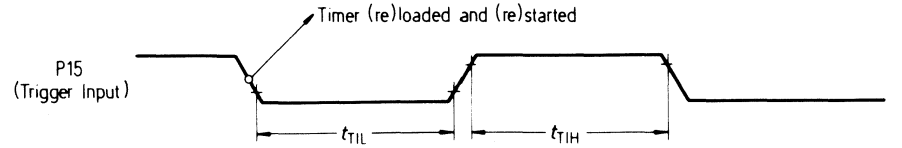
Count Pulse Timings and Zero-Crossing of Counter



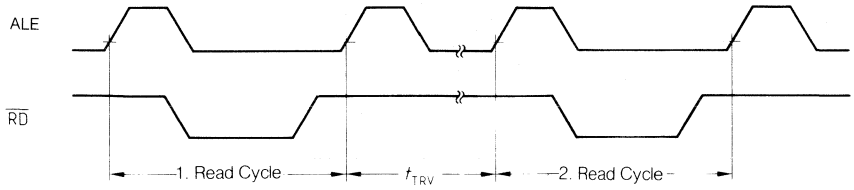
Loading Timer 5 (or Cascaded Counter/Timer 3 and 5) and Zero-Crossing of Counters (Cascaded Counter/Timer 3 and 5)



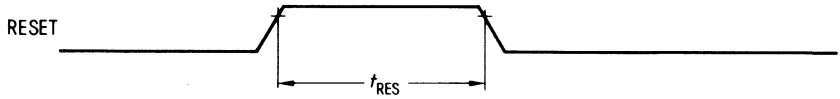
Trigger Pulse for Timer 5 (Cascaded Event Counter/Timer 3 and 5)



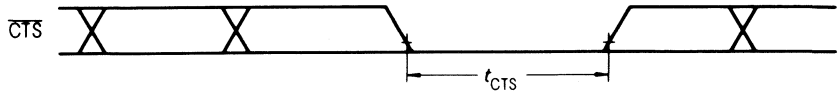
Reading event counters/timers



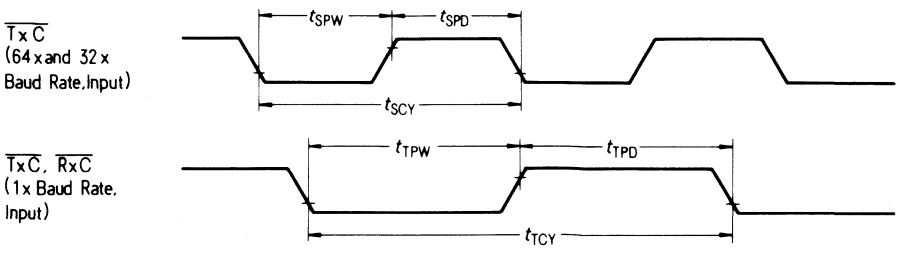
Reset Timing



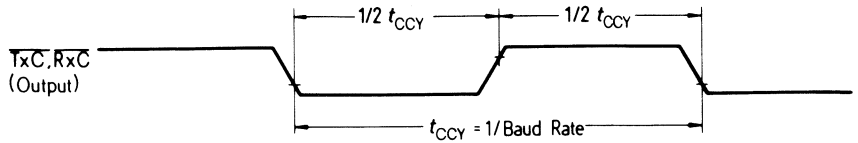
$\overline{CTS}$ for Single Character Transmission



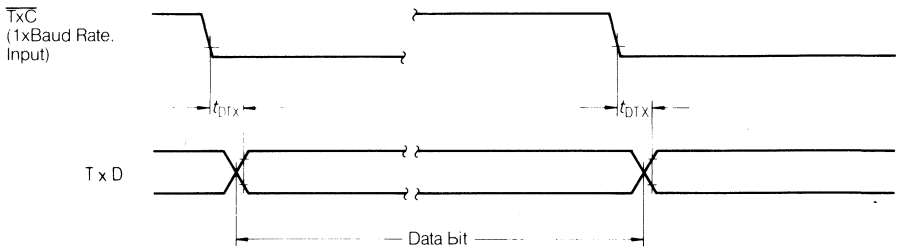
External Baud Rate Clock for Serial Interface



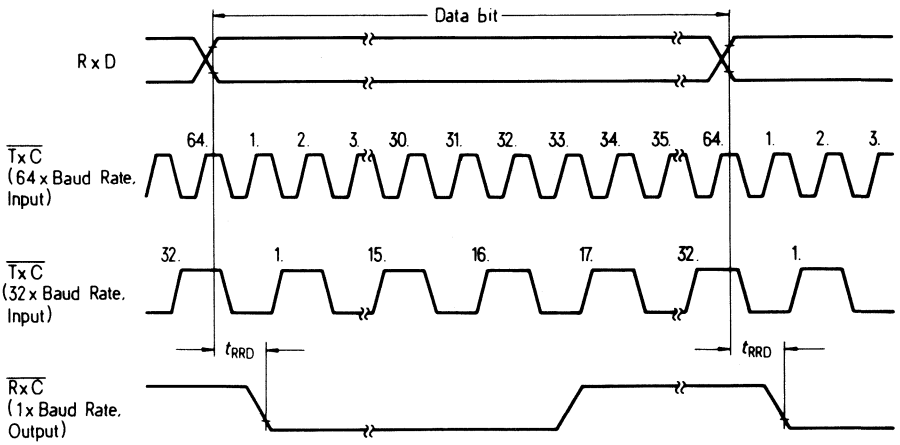
Transmitter and Receiver Clock from Internal Clock Source



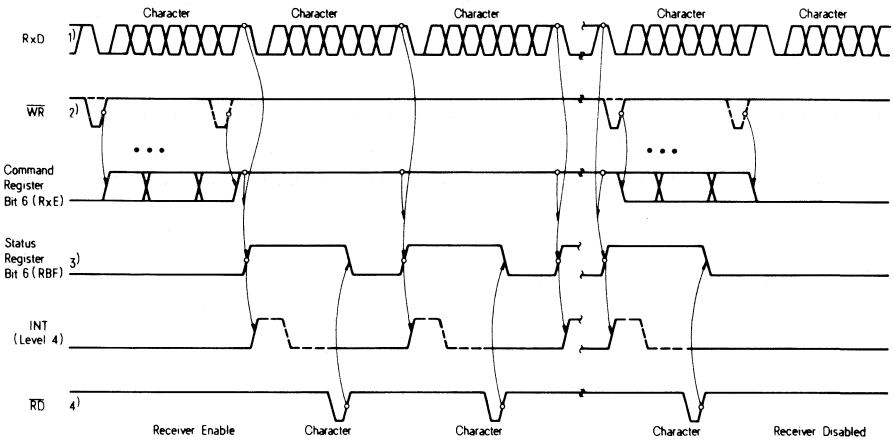
Data Bit Output on Serial Interface



Data Bit Input on Serial Interface



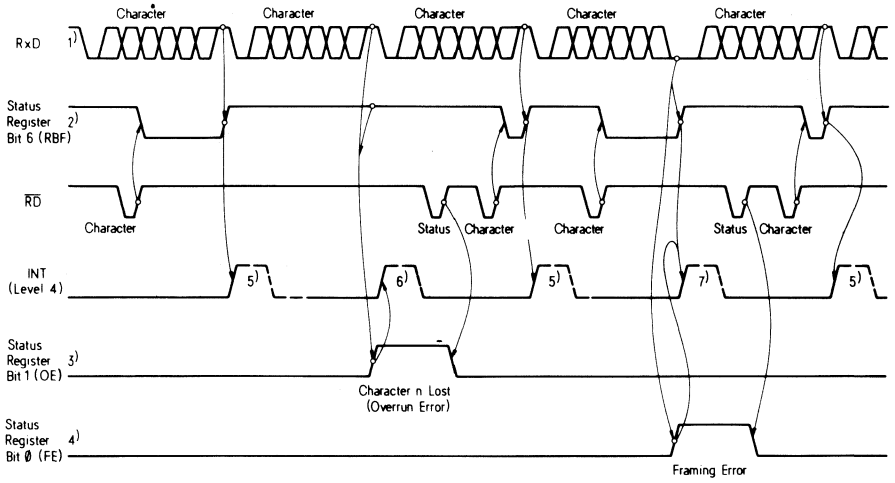
Continuous Reception of Characters on Serial Interface without error conditions



1) Character format for this example: 6 Data bits with Parity bit and one Stop bit.
2) Set or Reset bit 6 of Command Register 3 (Enable Receiver)
3) Receiver Buffer Loaded
4) Read Receiver Buffer Register
5) Receiver is active even though no data is sent or Status bit set.

No Status bits are altered when $\overline{RD}$ is active.

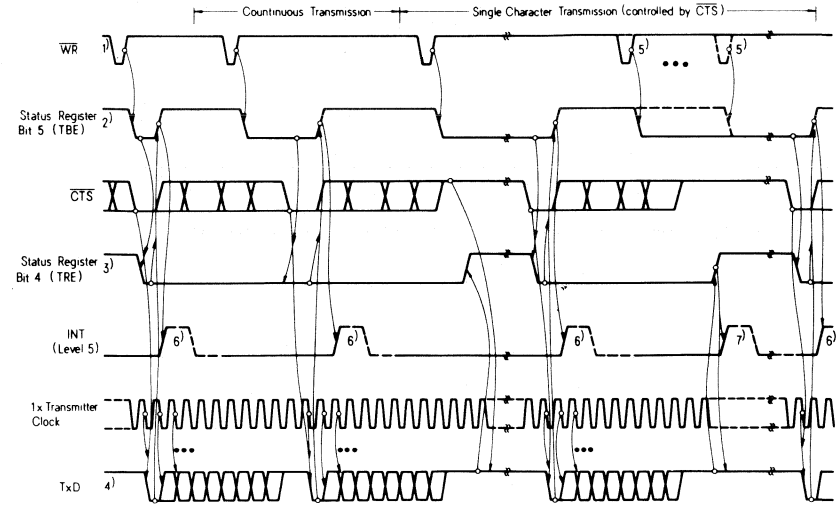
Error Conditions during Reception of Characters on the Serial Interface



1) Character format for this example: 6 Data bits without Parity and one Stop bit
2) Receiver Buffer Register Loaded
3) Overrun error
4) Framing error
5) Interrupt from receiver buffer register loading
6) Interrupt from Overrun error
7) Interrupt from framing error and loading receiver buffer register

No Status bits are altered when $\overline{RD}$ is active.

Transmission of Characters on Serial Interface

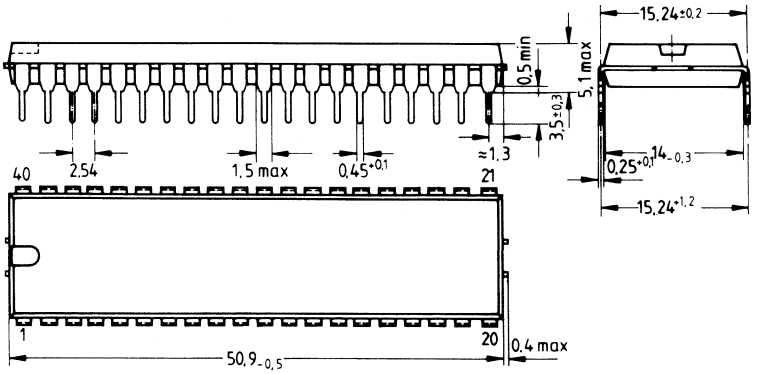


1) Load Transmitter buffer register
2) Transmitter buffer register is empty
3) Transmitter register is empty
4) Character format for this example: 7 Data bits with Parity bit and 2 Stop bits
5) Loading of transmitter buffer register must be completed before $\overline{CTS}$ goes low
6) Interrupt due to transmitter buffer register empty
7) Interrupt due to transmitter register empty

No Status bits are altered when $\overline{RD}$ is active.

Package Outline

40 Pin Plastic Package Type P



Ordering Information

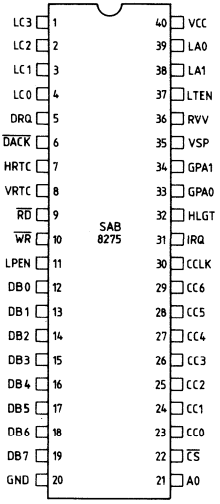
Type	Description	Ordering code
	Programmable Multifunction Chip MUART	
SAB 8256A–P	3 MHz system clock (plastic)	Q 67120-Y43
SAB 8256A–2–P	5 MHz system clock (plastic)	Q 67120-Y59

Preliminary

SAB 8275
Programmable CRT Controller

- Programmable screen and character format
- 6 independent visual field attributes
- 11 visual character attributes (graphics capability)
- Cursor control (4 types)
- Light pen detection and registers
- SAB 8051, SAB 8085, SAB 8086 and SAB 8088 compatible
- Dual row buffers
- Programmable DMA burst mode
- Single +5V supply
- High performance MYMOS technology
- Fully compatible with industry standard 8275

Pin configuration



Pin Names

LC0–LC3	Line Count
DRQ	DMA Request
DACK	DMA Acknowledge
HRTC	Horizontal Retrace
VRTC	Vertical Retrace
RD	Read Input
WR	Write Input
LPEN	Light Pen
DB0–DB7	Bidirectional Three-State Data Bus Lines
LA0, LA1	Line Attribute Codes
LTEN	Light Enable
RVV	Reverse Video
VSP	Video Suppression
GPA0, GPA1	General Purpose Attribute Codes
HLGT	Highlight
IRQ	Interrupt Request
CCLK	Character Clock
CC0–CC6	Character Codes
CS	Chip Select
A0	Port Address

The SAB 8275 programmable CRT controller is a single chip device to interface CRT raster scan displays. It is manufactured in Siemens advanced MYMOS technology. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the SAB 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

2.85

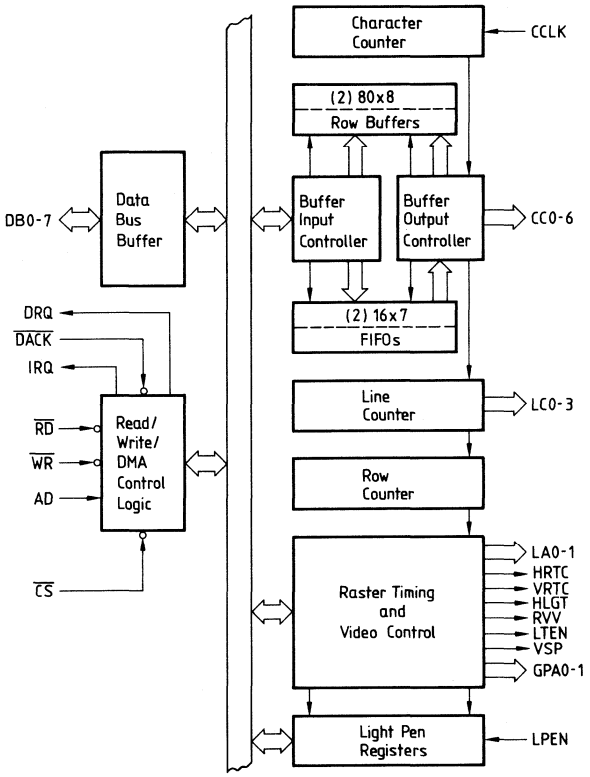
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
LC3 LC2 LC1 LC0	1 2 3 4	O	LINE COUNT: Output from the line counter which is used to address the character generator for the line positions on the screen.
DRQ	5	O	DMA REQUEST: Output signal to the SAB 8237A DMA controller requesting a DMA cycle.
$\overline{\text{DACK}}$	6	I	DMA ACKNOWLEDGE: Input signal from the SAB 8237A DMA controller acknowledging that the requested DMA cycle has been granted.
HRTC	7	O	HORIZONTAL RETRACE: Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
VRTC	8	O	VERTICAL RETRACE: Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
$\overline{\text{RD}}$	9	I	READ INPUT: A control signal to read registers.
$\overline{\text{WR}}$	10	I	WRITE INPUT: A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
LPEN	11	I	LIGHT PEN: Input signal from the CRT system signifying that a light pen signal has been detected.
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL THREE-STATE DATA BUS LINES: The outputs are enable during a read of the C or P ports.
LA0 LA1	39 38	O	LINE ATTRIBUTE CODES: These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
LTEN	37	O	LIGHT ENABLE: Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
RVV	36	O	REVERSE VIDEO: Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
VSP	35	O	VIDEO SUPPRESSION: Output signal used to blank the video signal to the CRT. This output is active: – During the horizontal and vertical retrace intervals. – at the top and bottom lines of rows if underline is programmed to be number 8 or greater. – when an end of row or end of screen code is detected. – when a DMA underrun occurs. – at regular intervals (1/16 frames frequency for cursor, 1/32 frame frequency for character and field attributes) – to create blinking displays as specified by cursor, character attribute, or field attribute programming.
GPA1, GPA0	34 33	O	GENERAL-PURPOSE ATTRIBUTE CODES: Outputs which are enable by the general purpose field attribute codes.
HLGT	32	O	HIGHLIGHT: Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
IRQ	31	O	INTERRUPT REQUEST.
CCLK	30	I	CHARACTER CLOCK (from dot/timing logic).
CC6 CC5 CC4 CC3 CC2 CC1 CC0	29 28 27 26 25 24 23	O	CHARACTER CODES: Output from the row buffers used for character selection in the character generator.
$\overline{CS}$	22	I	CHIP SELECT: The read and write are enabled by $\overline{CS}$.
A0	21	I	PORT ADDRESS: A high input on A0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
VCC	40	–	+5 V Power supply.
GND	20	–	Ground (0V)

SAB 8275 Block diagram showing counter and register functions



Functional Description

Data bus buffer

This three-state, bidirectional, 8-bit buffer is used to interface the SAB 8275 to the system data bus.

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the command, parameter, and status registers that store various control formats for the device functional definition.

A0	Operation	Register
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	1	0	0	Write SAB 8275 parameter
0	0	1	0	Read SAB 8275 parameter
1	1	0	0	Write SAB 8275 command
1	0	1	0	Read SAB 8275 status
X	1	1	0	Three-state
X	X	X	1	Three-state

$\overline{RD}$ (Read)

A "low" on this input informs the SAB 8275 that the CPU is reading data or status information from the SAB 8275.

$\overline{WR}$ (Write)

A "low" on this input informs the SAB 8275 that the CPU is writing data or control words to the SAB 8275.

$\overline{CS}$ (Chip select)

A "low" on this input selects the SAB 8275. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the data bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

DRQ (DMA request)

A "high" on this output informs the DMA controller that the SAB 8275 desires a DMA transfer.

$\overline{DACK}$ (DMA acknowledge)

A "low" on this input informs the SAB 8275 that a DMA cycle is in progress.

IRQ (Interrupt request)

A "high" on this output informs the CPU that the SAB 8275 desires interrupt service.

Character counter

The character counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (character clock) input, which should be a derivative of the external dot clock.

Line counter

The line counter is a programmable counter that is used to determine the number of horizontal lines (sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row counter

The row counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light pen registers

The light pen registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

Note: Software correction is required.

Raster timing and video controls

The raster timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The video control circuitry controls the generation of LA0–1 (line attribute), HGLT (highlight), RVV (reverse video), LTEN (Light enable), VSP (video suppress), and GPA0–1 (general purpose attribute) outputs.

Row buffers

The row buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

FIFOs

There are two 16 character FIFOs in the 8275. They are used to provide extra row buffer length in the transparent attribute mode.

Buffer input/output controllers

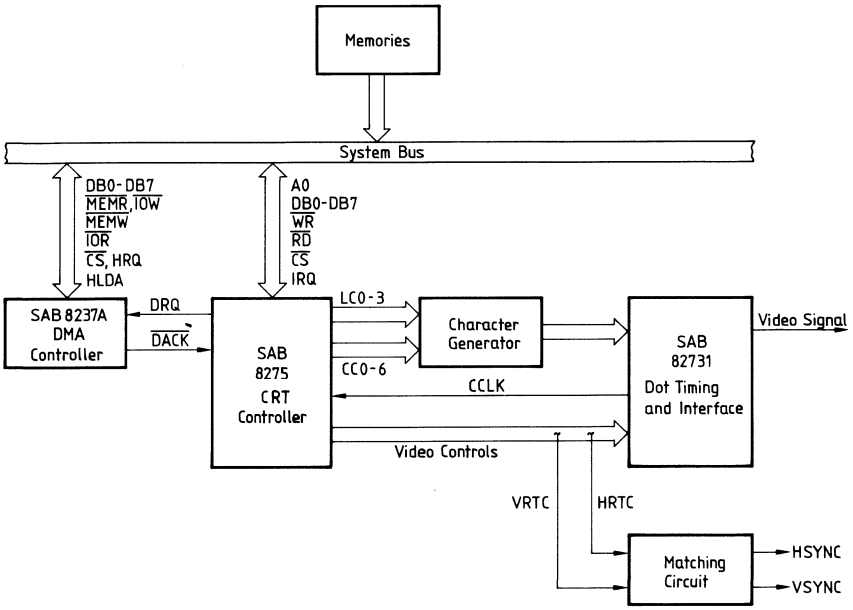
The buffer input/output controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action (Examples: An "end of screen-stop DMA" special code will cause the buffer input controller to stop further DMA requests. A "highlight" field attribute will cause the buffer output controller to activate the HGLT output).

System Operation

The SAB 8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with the SAB 8237A DMA controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

SAB 8275 Block diagram showing systems operation



Raster timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace (programmable from 2 to 32). This is constantly repeated.

The line counter is driven by the character counter. It is used to generate the line address outputs (LC0–3) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

The video suppression output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT display.

DMA timing

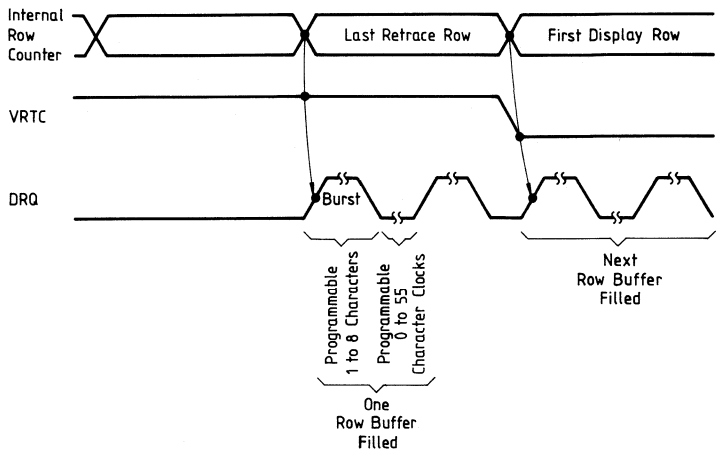
The SAB 8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods ±1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the SAB 8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

The DMA request for a row will start at the first character clock of the preceding row. If the burst mode is used, the first DMA request may occur a number of character clocks later. This number is equal to the programmed burst space.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

DMA timing

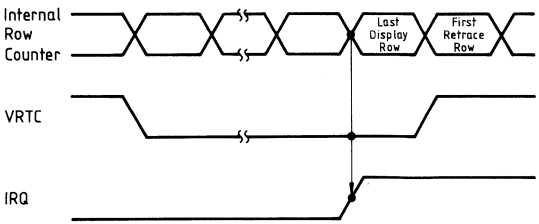


The DMA controller is typically initialized for the next frame at the end of the current frame.

Interrupt timing

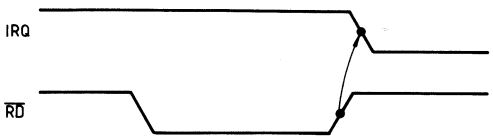
The SAB 8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the SAB 8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row.*

Beginning of interrupt request



IRQ will go inactive after the status register is read.

End of interrupt request



A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the SAB 8275 interrupt enable flag should not be set.

Note: Upon power-up, the SAB 8275 interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the SAB 8275 before system interrupts are enabled.

General systems operational description

The SAB 8275 provides a "window" into the microcomputer system memory.

Display characters are retrieved from memory and displayed on a row by row basis. The SAB 8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (see programming section.)

The SAB 8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See programming section.)

The SAB 8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See programming section.)

The SAB 8275 provides special control codes which can be used to minimize DMA or software overhead. It also provides visual attribute codes to cause special action or symbols on the screen without the use of the character generator (see visual attribute section).

The SAB 8275 also controls raster timing. This is done by generating horizontal retrace (HRTC) and vertical retrace (VRTC) signals. The timing of these signals is programmable.

The SAB 8275 can generate a cursor. Cursor location and format are programmable. (See programming section.)

The SAB 8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See programming section.)

Display row buffering

Before the start of a frame, the SAB 8275 requests DMA and one row buffer is filled with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

This is repeated until all of the character rows are displayed.

Screen format

The SAB 8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

The SAB 8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

Row format

The SAB 8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by line counter.

Mode 0 is use ful for character generators that leave address zero blank and start at address 1, Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

If the line *number* underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (light enable) signal.

Dot format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

Visual Attributes and Special Codes

The characters processed by the SAB 8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The most significant bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

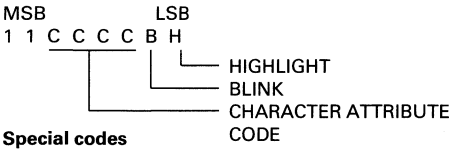
There are two types of visual attribute codes. They are character attributes and field attributes.

Character attribute codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the line attribute outputs (LA0–1), the video suppression output (VSP), and the light enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the video suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the highlight output (HGLT).

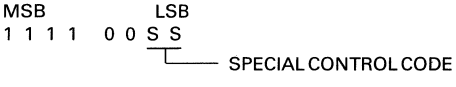
Character attributes



Special codes

Four special codes are available to help reduce memory, software or DMA overhead.

Special control character



S S	Function
0 0	End of Row
0 1	End of Row-stop DMA
1 0	End of Screen
1 1	End of Screen-stop DMA

The End-of-Row code (00) activates VSP and holds it to the end of the line.

The End-of-Row-Stop DMA code (01) causes the DMA control logic to stop DMA for the rest of the row when it is written into the row buffer. It affects the display in the same way as the end-of-row code (00).

The end-of-screen code (10) activates VSP and holds it to the end of the frame.

The end-of-screen-stop DMA code (11) causes the DMA control logic to stop DMA for the rest of the frame when it is written into the row buffer. It affects the display in the same way as the end-of-screen code (10).

If the stop DMA feature is not used, all characters after an end-of-row character are ignored, except for the end-of-screen character, which operates normally. All characters after an end-of-screen character are ignored.

Note: If a stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the stop DMA character.

Field attributes

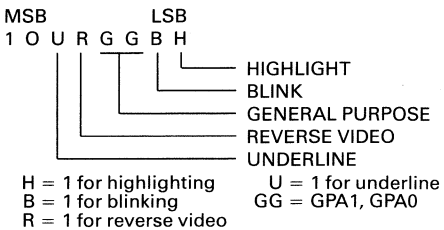
The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* – Characters following the code are caused to blink by activating the Video Suppression Output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* – Characters following the code are caused to be highlighted by activating the Highlight Output (HGLT).
3. *Reverse Video* – Characters following the code are caused to appear with reverse video by activating the Reverse Video Output (RVV).
4. *Underline* – Characters following the code are caused to be underlined by activating the Light Enable Output (LTEN).

5, 6. *General Purpose* – There are two additional SAB 8275 outputs which act as general purpose, independently programmable field attributes. GPA0–1 are active high outputs.

Field attribute code



* More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

The SAB 8275 can be programmed to provide visible or invisible field attribute characters.

If the SAB 8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the video suppression output (VSP). The chosen visual attributes are activated after this blanked character.

If the SAB 8275 is programmed in the invisible field attribute mode, the SAB 8275 FIFO is activated.

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the next character in the proper FIFO.

When a field attribute is placed in the buffer output controller during display, it causes the controller to immediately put a character from the FIFO on the character code outputs (CC0–8). The chosen visual attributes are also activated.

Since the FIFO in 16 characters long, no more then 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

Note: Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a visual attribute or special code must *not* immediately follow a field attribute code. If this situation does occur, the visual attribute or special code will be treated as normal display character.

Field and character attribute interaction

Character attribute symbols are affected by the reverse video (RVV) and general purpose (GPA0–1) field attributes. They are not affected by underline, blink or highlight field attribute; however, these characteristics can be programmed *individually* for character attribute symbols.

Cursor timing

The cursor location is determined by a cursor row register and a character position register which are located by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light pen detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enable the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the SAB 8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

Note: Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device programming

The SAB 8275 has two programming registers, the command register (CREG) and the parameter register (PREG). It also has a status register (SREG). The command register can only be written into and the Status registers can only be read from. They are addressed as follows:

A_0	operation	register
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The SAB 8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The SAB 8275 instruction set consists of 8 commands.

Command	No. of parameter bytes
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the SAB 8275 (SREG) can be read by the CPU at any time.

1 Reset command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Reset command	0 0 0 0 0 0 0 0
Parameters	Write	0	Screen Comp Byte 1	S H H H H H H H
	Write	0	Screen comp Byte 2	V V R R R R R R
	Write	0	Screen comp Byte 3	U U U U L L L L
	Write	0	Screen comp Byte 4	M F C C Z Z Z Z

Action – After the reset command is written, DMA requests stop, SAB 8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter – S Spaced rows

S	Functions
0	Normal rows
1	Spaced Rows

Parameter – HHHHHHH Horizontal characters/row

H H H H H H H	No. of characters per row
0 0 0 0 0 0 0	1
0 0 0 0 0 0 1	2
0 0 0 0 0 1 0	3
. . .	.
. . .	.
. . .	.
1 0 0 1 1 1 1	80
1 0 1 0 0 0 0	Undefined
. . .	.
. . .	.
. . .	.
1 1 1 1 1 1 1	Undefined

Parameter – VV Vertical retrace row count

V V	No. of row counts per VRTC
0 0	1
0 1	2
1 0	3
1 1	4

Parameter – RRRRRR Vertical rows/frame

R R R R R R	No. of rows/frame
0 0 0 0 0 0	1
0 0 0 0 0 1	2
0 0 0 0 1 0	3
. . .	.
. . .	.
. . .	.
1 1 1 1 1 1	64

Parameter – UUUU Underline placement

U U U U	Line number of underline
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
. . .	.
. . .	.
. . .	.
1 1 1 1	16

Note: uuuu MSB determines blanking of top and botton lines (1 = blanked, 0 = not blanked).

Parameter – LLLL Number of lines per character row

L	L	L	L	No. of lines/row
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter – ZZZZ Horizontal retrace count

Z	Z	Z	Z	No. of character counts per HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

Parameter – M Line Counter Mode

M	Line counter mode
0	Mode 0 (non-offset)
1	Mode 1 (offset by 1 count)

Parameter – F Field attribute mode

F	Field attribute mode
0	Transparent
1	Non-transparent

Parameter – CC Cursor format

C	C	Cursor format
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underling

2 Start display command

	Operation	A0	Description	Data bus MSB							LSB
Command	Write	1	Start display	0	0	1	S	S	S	B	B
No parameters											

SSS Burst space code

S	S	S	No. of character clocks between DMA requests
0	0	0	0
0	0	1	7
0	1	0	15
0	1	1	23
1	0	0	31
1	0	1	39
1	1	0	47
1	1	1	55

BB Burst count code

B	B	No. of DMA cycles per burst
0	0	1
0	1	2
1	0	4
1	1	8

Action – SAB 8275 interrupts are enabled, DMA requests begin, video is enabled, interrupt enable and video enable status flags are set.

3 Stop display command

	Operation	A0	Description	Data bus MSB							LSB
Command	Write	1	Stop display	0	1	0	0	0	0	0	0
No parameters											

Action – Disables video, interrupts remain enabled. HRTC and VRTC continue to run, video enable status flag is reset, and the "Start display" command must be given to re-enable the display.

4 Read light pen command

	Operation	A0	Description	Data bus MSB							LSB
Command	Write	1	read light pen	0	1	1	0	0	0	0	0
Parameters	Read	0	Char. number	(Char. position in row)							
	Read	0	Row number	(Row number)							

Action – The SAB 8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

Note: Software correction of light pen position is required.

5 Load cursor position

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Load cursor	1 0 0 0 0 0 0 0
Parameters	Write	0	Char. number	(Char. position in row)
	Write	0	Row number	(Row number)

Action – The SAB 8275 is conditioned to place, the next two parameter bytes into the cursor position registers. Status flags not affected.

6 Enable interrupt command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Enable interrupt	1 0 1 0 0 0 0 0
No parameters				

Action – The interrupt enable status flag is set and interrupts are enabled.

7 Disable interrupt command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Disable interrupt	1 1 0 0 0 0 0 0
No parameters				

Action – Interrupts are disabled and the interrupt enable status flag is reset.

8 Preset counters command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Preset counters	1 1 1 0 0 0 0 0
No parameters				

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU. After this command, two additional clock cycles are required before the first character of the first row is put out.

Status flags

	Operation	A0	Description	Data bus MSB LSB
Command	Read	1	Status word	0 IE IR LP IC VE DU F0

IE – (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command reset with the "Reset" command.

IR – (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP – This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC – (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE – (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU – (DMA Underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO – (FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

Absolute Maximum Ratings [1)]

Temperature under bias	0 to +70 °C
Storage temperature	−65 to +150 °C
All output ans supply and supply voltages	−0,5 to +7 V
All input voltages	−0,5 to +5,5 V
Power dissipation	1,0 W

DC Characteristics

(TA = 0°C to 70°C, VCC = 5 V ±5%)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC+0.5V		
VOL	Output low voltage	–	0.45		IOL = 2.2 mA
VOH	Output high voltage	2.4	–		IOH = −400 µA
IIL	Input load current	–	±10	µA	VIN = VCC to 0 V
IOFL	Output float leakage				VOUT = VCC to 0.45 V
ICC	VCC supply current		160	mA	–

Capacitance

(TA = 25°C, VCC = GND = 0 V)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
CIN	Input capacitance	–	10	pF	fc = 1 MHz
CI/O	I/O capacitance		20		Unmeasured pins returned to GND

1) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics (SAB 8275)

(TA = 0 C to 70°C, VCC = 5.0 V ± 5%, GND = 0 V)

Clock timing

Symbol	Parameter	Limit values		Units	Test condition
		Min.	Max.		
TCLK	Clock period	480	–	ns	–
TKH	Clock high	240			
TKL	Clock low	160			
TKR	Clock rise	5	30		
TKF	Clock fall				

Bus parameters
Read cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAR	Address stable before READ	0	–	ns	–
TRA	Address hold time for READ				
TRR	READ pulse width	250			
TRD	Data delay from READ	–	200		CL = 150 pF
TDF	READ to data floating		100		

Write cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAW	Address stable before WRITE	0	–	ns	–
TWA	Address hold time for WRITE				
TWW	WRITE pulse width	250			
TDW	Data seting time for WRITE	150			
TWD	Data hold time for WRITE	0			

Other timings

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCC	Character code output delay	–	150	ns	CL = 50 pF
THR	Horizontal retrace output delay		200		
TLC	Line count output delay		400		
TAT	Control-attribute output delay		275		
TVR	Vertical retrace output delay				
TRI	IRQ↓ from RD↑		250		
TWQ	DRQ↑ from WR↑				
TRQ	DRQ↓ from WR↓		200		
TLR	DACK↓ to WR↓	0	–		–
TRL	WR↑ to DACK↑				
TPR	LPEN rise	–	50		
TPH	LPEN hold	100	–		

AC Characteristics (SAB 8275-2)

(TA = 0 C to 70°C, VCC = 5.0 V ± 5%, GND = 0 V)

Clock timing

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCLK	Clock period	320	–	ns	–
TKH	Clock high	120			
TKL	Clock low				
TKR	Clock rise	5	30		
TKF	Clock fall				

Bus parameters
Read cycle

Symbol	Parameter	Limit value		Unit	Test condition
		Min.	Max.		
TAR	Address stable before READ	0	–	ns	–
TRA	Address hold time for READ				
TRR	READ pulse width	250			
TRD	Data delay from READ	–	200		CL = 150 pF
TDF	READ to data floating		100		CL = 150 pF

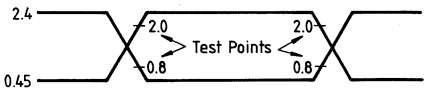
Write cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAW	Address stable before WRITE	0	–	ns	–
TWA	Address hold time for WRITE				
TWW	WRITE pulse width	250			
TDW	Data seting time for WRITE	150			
TWD	Data hold time for WRITE	0			

Other timings

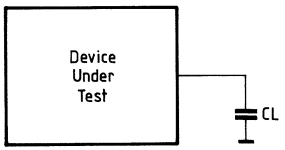
Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCC	Character code output delay	–	150	ns	CL = 50 pF
THR	Horizontal retrace output delay				
TLC	Line count output delay		250		
TAT	Control-attribute output delay				
TVR	Vertical retrace output delay				
TRI	IRQ↓ from RD↑				
TWQ	DRQ↑ from WR↑				
TRQ	DRQ↓ from WR↓		200		
TLR	DACK↓ to WR↓	0	–		–
TRL	WR↑ to DACK↑				
TPR	LPEN rise	–	50		
TPH	LPEN hold	100	–		

A.C. Testing input/output



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

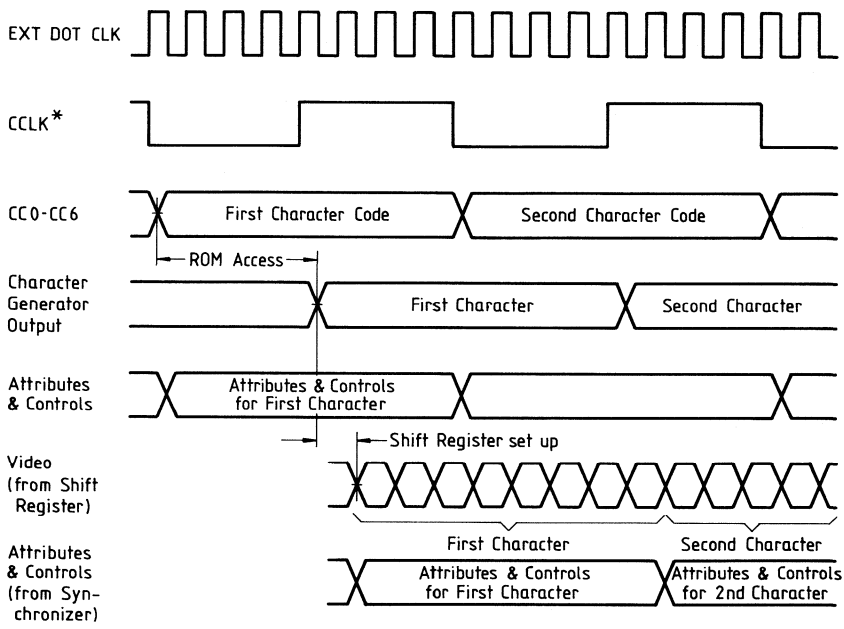
A.C. Testing load circuit



CL Includes Jig Capacitance

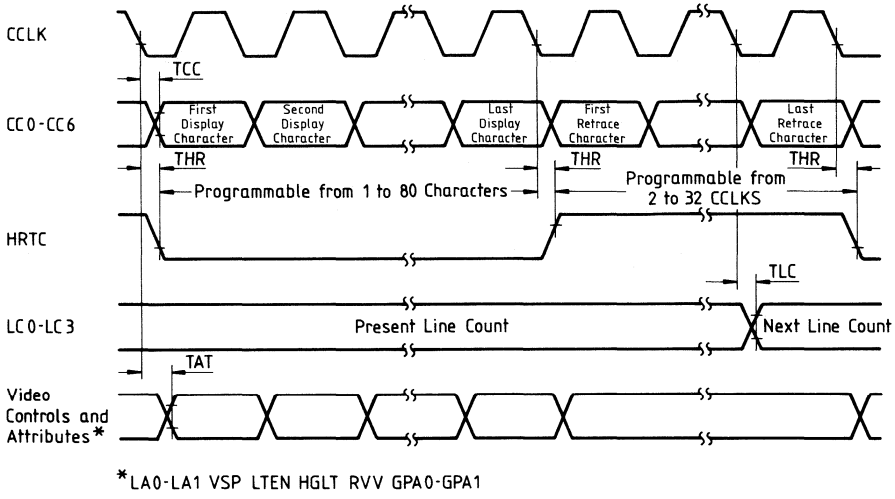
Waveforms

Typical dot level timing



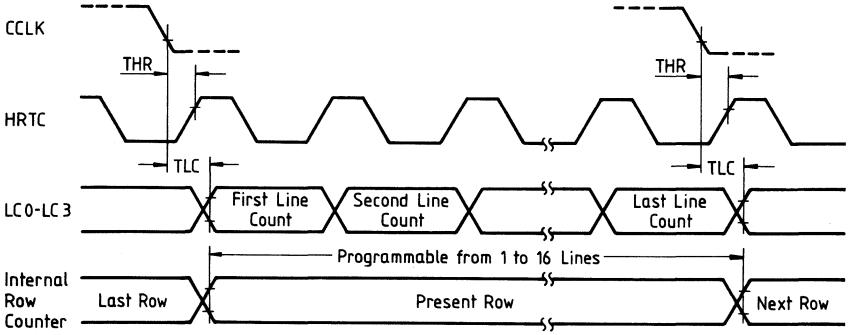
*CCLK is a Multiple of the Dot Clock and an Input to the SAB 8275

Line timing

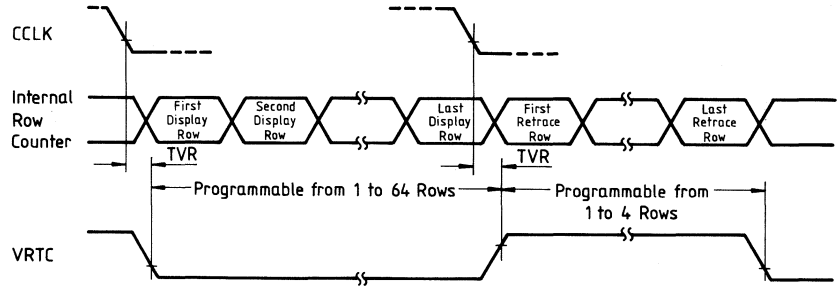


*LA0-LA1 VSP LTEN HGLT RVV GPA0-GPA1

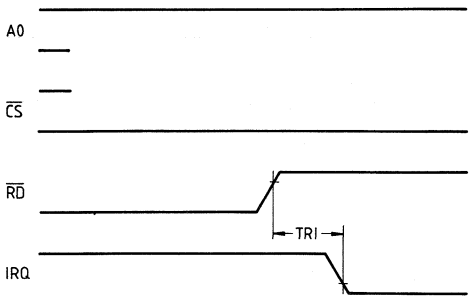
Row timing



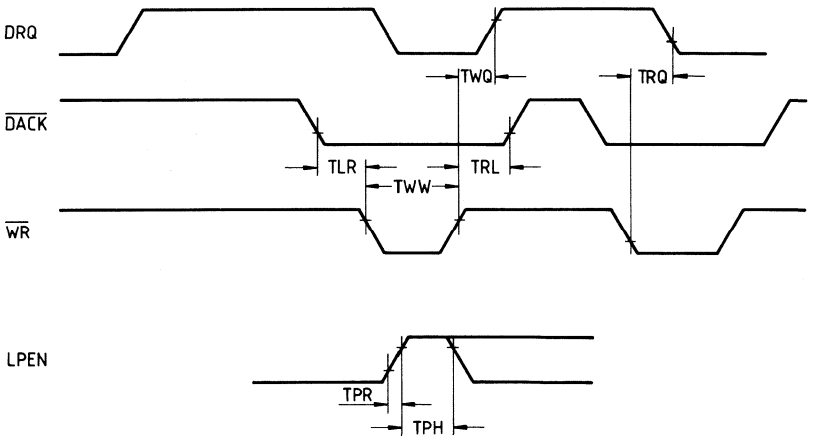
Frame timing



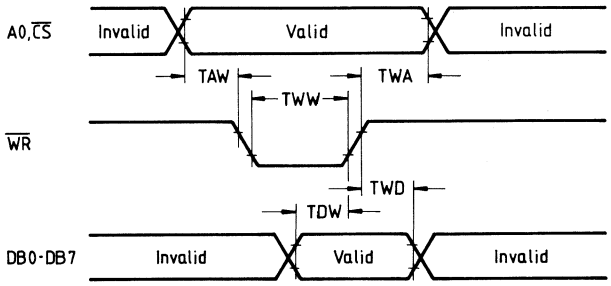
Interrupt timing



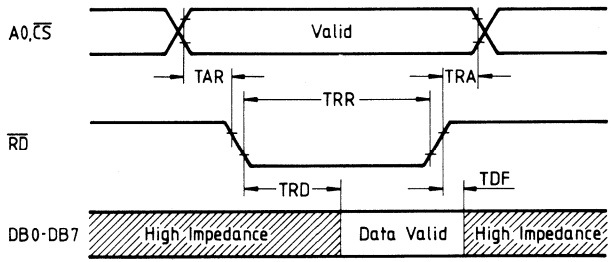
DMA timing



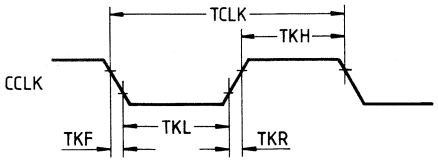
Write timing



Read timing

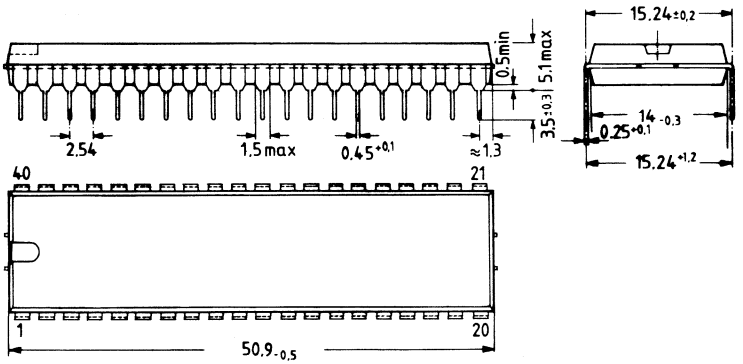


Clock timing



Package outline

40 Pin plastic package – Type P



Ordering Information

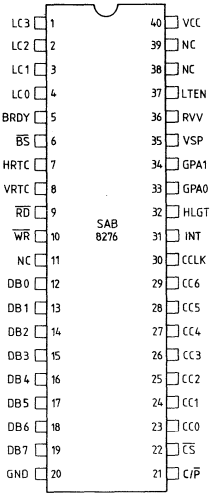
Type	Description	Ordering code
SAB 8275-P	Programmable CRT controller, 2 MHz	Q67120-P58
SAB 8275-2-P	Programmable CRT controller, 3 MHz	Q67120-P92

Preliminary

SAB 8276
Small System CRT Controller

- Programmable screen and character format
- 6 independent visual attributes
- Cursor control (4 types)
- SAB 8051, SAB 8085, SAB 8086 and SAB 8088 compatible
- Dual row buffers
- Programmable DMA burst mode
- Single +5V supply
- High performance MYMOS technology
- Fully compatible with industry standard 8276

Pin configuration



Pin Names

LC0–LC3	Line Count
BRDY	Buffer Ready
$\overline{BS}$	Buffer Select
HRTC	Horizontal Retrace
VRTC	Vertical Retrace
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
DB0–DB7	Bidirectional Three-State Data Bus Lines
LTEN	Light Enable
RVV	Reverse Video
VSP	Video Suppression
GPA0, GPA1	General Purpose Attribute Codes
HLGT	Highlight
INT	Interrupt Output
CCLK	Character Clock
CC0–CC6	Character Codes
$\overline{CS}$	Chip Select
C/$\overline{P}$	Port Address

The SAB 8276 Small System CRT Controller is a single chip device to interface CRT raster scan displays. It is manufactured in Siemens advanced MYMOS technology. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the SAB 8276 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

11.86

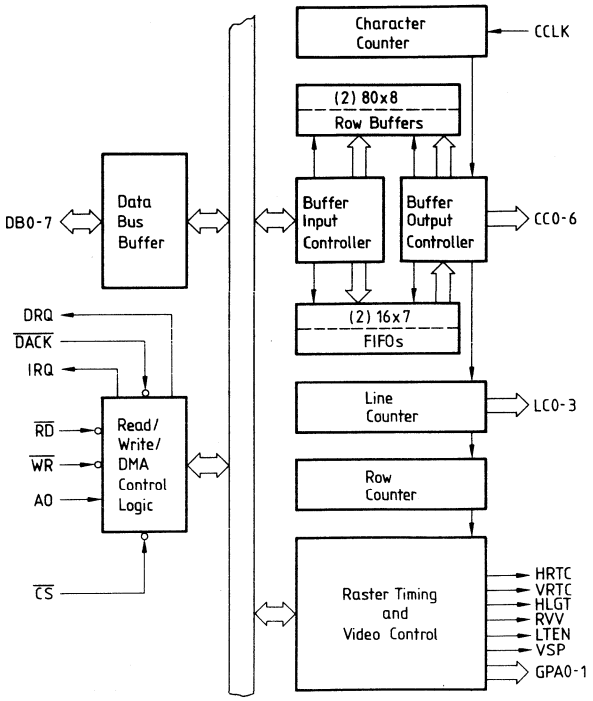
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
LC3 LC2 LC1 LC0	1 2 3 4	O	LINE COUNT: Output from the line counter which is used to address the character generator for the line positions on the screen.
BRDY	5	I	BUFFER READY: Output signal indicating that a row buffer is ready for loading of character data.
$\overline{BS}$	6	O	BUFFER SELECT: Input signal enabling $\overline{WR}$ for character data into the row buffers.
HRTC	7	O	HORIZONTAL RETRACE: Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
VRTC	8	O	VERTICAL RETRACE: Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
$\overline{RD}$	9	I	READ INPUT: A control signal to read registers.
$\overline{WR}$	10	I	WRITE INPUT: A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
NC	11		No Connection
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL THREE-STATE DATA BUS LINES: The outputs are enable during a read of the C or P ports.
NC	38/39		No Connection
LTEN	37	O	LIGHT ENABLE: Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
RVV	36	O	REVERSE VIDEO: Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
VSP	35	O	VIDEO SUPPRESSION: Output signal used to blank the video signal to the CRT. This output is active: – During the horizontal and vertical retrace intervals. – at the top and bottom lines of rows if underline is programmed to be number 8 or greater. – when an end of row or end of screen code is detected. – when a DMA underrun occurs. – at regular intervals (1/16 frames frequency for cursor, 1/32 frame frequency for character and field attributes) – to create blinking displays as specified by cursor or field attribute programming.
GPA1 GPA0	34 33	O	GENERAL-PURPOSE ATTRIBUTE CODES: Outputs which are enable by the general purpose field attribute codes.
HLGT	32	O	HIGHLIGHT: Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
INT	31	O	INTERRUPT OUTPUT
CCLK	30	I	CHARACTER CLOCK (from dot/timing logic).
CC6 CC5 CC4 CC3 CC2 CC1 CC0	29 28 27 26 25 24 23	O	CHARACTER CODES: Output from the row buffers used for character selection in the character generator.
$\overline{CS}$	22	I	CHIP SELECT: The read and write are enabled by $\overline{CS}$.
C/$\overline{P}$	21	I	PORT ADDRESS: A high input on C/$\overline{P}$ selects "C" port or command registers and a low input selects the "P" port or parameter registers.
VCC	40	–	+5 V Power supply.
GND	20	–	Ground (0V)

SAB 8276 Block diagram showing counter and register functions



Functional Description

Data bus buffer

This three-state, bidirectional, 8-bit buffer is used to interface the SAB 8276 to the system data bus.

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the command, parameter, and status registers that store various control formats for the device functional definition.

C/$\overline{P}$	Operation	Register
0	Read	Reserved
0	Write	Parameter
1	Read	STATUS
1	Write	COMMAND

C/$\overline{P}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	$\overline{BS}$	
0	0	1	0	1	Reserved
0	1	0	0	1	Write 8276 Parameter
1	0	1	0	1	Read 8276 Status
1	1	0	0	1	Write 8276 Command
X	1	0	1	0	Write 8276 Row Buffer
X	1	1	X	X	High Impedance
X	X	X	1	1	High Impedance

$\overline{RD}$ (Read)

A "low" on this input informs the SAB 8276 that the CPU is reading data or status information from the SAB 8276.

$\overline{WR}$ (Write)

A "low" on this input informs the SAB 8276 that the CPU is writing data or control words to the SAB 8276.

$\overline{CS}$ (Chip select)

A "low" on this input selects the SAB 8276. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the data bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

BRDY (BUFFER READY)

A "high" on this output indicates that the SAB 8276 is ready to receive character data.

$\overline{BS}$ (BUFFER SELECT)

A "low" on this input enables $\overline{WR}$ of character data to the SAB 8276 row buffers.

INT (Interrupt Output)

A "high" on this output informs the CPU that the SAB 8276 desires interrupt service.

Character counter

The character counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (character clock) input, which should be a derivative of the external dot clock.

Line counter

The line counter is a programmable counter that is used to determine the number of horizontal lines (sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row counter

The row counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Raster timing and video controls

The raster timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The video control circuitry controls the generation of HGLT (highlight), RVV (reverse video), LTEN (Light enable), VSP (video suppress), and GPA0–1 (general purpose attribute) outputs.

Row buffers

The row buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

Buffer input/output controllers

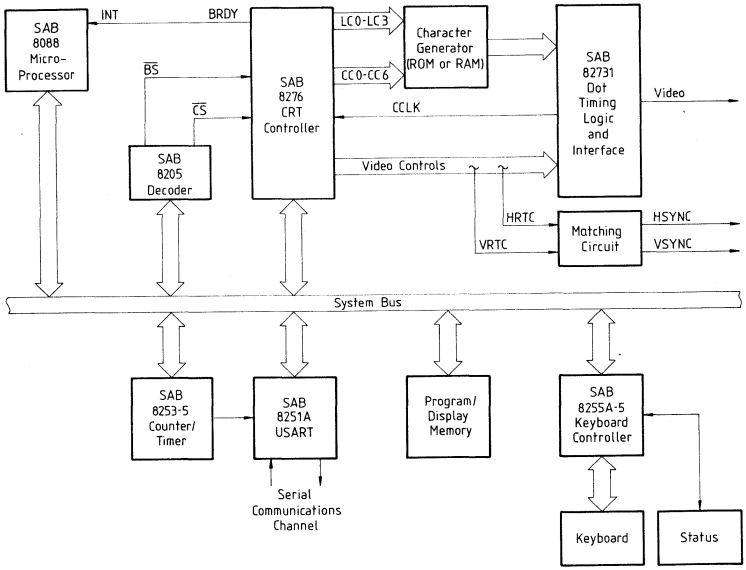
The buffer input/output controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action (Examples: A "HIGHLIGHT" attribute will cause the Buffer Output Controller to activate the HGLT output).

System Operation

The SAB 8276 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with standard character generator for dot matrix decoding.
Dot level must be provided by external circuitry.

SAB 8276 Block diagram showing systems operation



Raster timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then cause the line counter to increment, and it starts counting out the horizontal retrace (programmable from 2 to 32). This is constantly repeated.

The line counter is driven by the character counter. It is used to generate the line address outputs (LC0–3) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

The video suppression output (VSP) is active during horizontal and vertical retrace intervals.

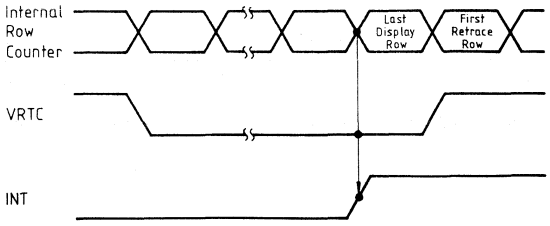
Dot level timing circuitry must synchronize these outputs with the video signal to the CRT display.

Interrupt timing

The SAB 8276 can be programmed to generate an interrupt request at the end of each frame.

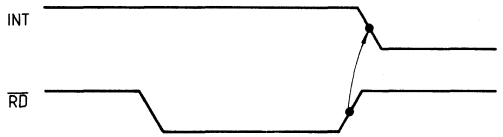
If the SAB 8276 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.

Beginning of interrupt request



IRQ will go inactive after the status register is read.

End of interrupt



A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Note: Upon power-up, the SAB 8276 interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the SAB 8276 before system interrupts are enabled.

Generalsystems operational description

Display characters are retrieved from memory and displayed on a row by row basis. The SAB 8276 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays (see programming section).

The SAB 8276 uses BRDY to request data to fill the row buffer that is not being used for display. The SAB 8276 displays character rows one line at a time. The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable (see programming section).

The SAB 8276 provides special control codes which can be used to minimize overhead. It also provides visual attribute codes to cause special action on the screen without the use of the character generator (see visual attribute section).

The SAB 8276 also controls raster timing. This is done by generating horizontal retrace (HRTC) and vertical retrace (VRTC) signals. The timing of these signals is programmable.

The SAB 8276 can generate a cursor. Cursor location and format are programmable (see programming section).

Display row buffering

Before the start of a frame, the SAB 8276 uses BRDY and $\overline{BS}$ to fill one row buffer with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, the other row buffer is filled with the next row of characters.

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

This is repeated until all of the character rows are displayed.

Screen format

The SAB 8276 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

The SAB 8276 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. Display data is not requested for the blanked rows.

Row format

The SAB 8276 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by line counter.

Mode 0 is useful for character generators that leave address zero blank and start at address 1, Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

If the line *number* underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (light enable) signal.

Dot format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

Visual Attributes and Special Codes

The characters processed by the SAB 8276 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The most significant bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

Special codes

Four special codes are available to help reduce memory, software or DMA overhead.

Special control character

MSB LSB
1 1 1 1 0 0 S S
SPECIAL CONTROL CODE

S S	Function
0 0	End of Row
0 1	End of Row-stop Buffer Loading
1 0	End of Screen
1 1	End of Screen-stop Buffer Loading

The end-of-row code (00) activates VSP and holds it to the end of the line.

The end-of-row Buffer Loading code (BRDY) causes the Buffer Loading control logic to stop Buffer Loading for the rest of the row when it is written into the row buffer. It affects the display in the same way as the end-of-row code (00).

The end-of-screen code (10) activates VSP and holds it to the end of the frame.

The end-of-screen-stop Buffer Loading code (BRDY) causes the Buffer Loading control logic to stop Buffer Loading for the rest of the frame when it is written into the row buffer. It affects the display in the same way as the end-of-screen code (10).

If the stop Buffer Loading feature is not used, all characters after an end-of-row character are ignored, except for the end-of-screen character, which operates normally. All characters after an end-of-screen character are ignored.

Note: If a stop Buffer Loading character is not the last character in a burst or row, Buffer Loading is not stopped until after the next character is read. In the situation, a dummy character must be placed in memory after the stop Buffer Loading character.

Field attributes

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* – Characters following the code are caused to blink by activating the Video Suppression Output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* – Characters following the code are caused to be highlighted by activating the Highlight Output (HGLT).
3. *Reverse Video* – Characters following the code are caused to appear with reverse video by activating the Reverse Video Output (RVV).
4. *Underline* – Characters following the code are caused to be underlined by activating the Light Enable Output (LTEN).

5, 6. *General Purpose* – There are two additional SAB 8276 outputs which act as general purpose, independently programmable field attributes. GPA0–1 are active high outputs.

Field attribute code

MSB LSB
1 O U R G G B H
HIGHLIGHT
BLINK
GENERAL PURPOSE
REVERSE VIDEO
UNDERLINE

H = 1 for highlighting
B = 1 for blinking
R = 1 for reverse video
U = 1 for underline
GG = GPA1, GPA0

* More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

Cursor timing

The cursor location is determined by a cursor row register and a character position register which are located by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Device programming

The SAB 8276 has two programming registers, the command register and the parameter register. It also has a status register. The command register can only be written into and the Status registers can only be read from. They are addressed as follows:

A_0	operation	register
0	Read	Reserved
0	Write	Parameter
1	Read	Status
1	Write	Command

The SAB 8276 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The SAB 8276 instruction set consists of 7 commands.

Command	No. of parameter bytes
Reset	4
Start Display	0
Stop Display	0
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the SAB 8276 can be read by the CPU at any time.

1 Reset command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Reset command	0	0	0	0	0	0	0	0
Parameters	Write	0	Screen comp Byte 1	S	H	H	H	H	H	H	H
	Write	0	Screen comp Byte 2	V	V	R	R	R	R	R	R
	Write	0	Screen comp Byte 3	U	U	U	U	L	L	L	L
	Write	0	Screen comp Byte 4	M	1	C	C	Z	Z	Z	Z

Action – After the reset command is written, BRDY goes inactive, SAB 8276 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up. As parameters are written, the screen composition is defined.

Parameter – S Spaced rows

S	Functions
0	Normal rows
1	Spaced rows

Parameter – HHHHHHH Horizontal characters/row

H	H	H	H	H	H	H	No. of characters per row
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
			.				.
			.				.
			.				.
1	0	0	1	1	1	1	80
1	0	1	0	0	0	0	Undefined
			.				.
			.				.
			.				.
1	1	1	1	1	1	1	Undefined

Parameter – VV Vertical retrace row count

V	V	No. of row counts per VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Parameter – LLLL Number of lines per character row

L	L	L	L	No. of lines/row
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter – M Line counter mode

M	Line counter mode
0	Mode 0 (non-offset)
1	Mode 1 (offset by 1 count)

Parameter – RRRRRR Vertical rows/frame

R	R	R	R	R	R	No. of rows/frame
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			.			.
			.			.
			.			.
1	1	1	1	1	1	64

Parameter – UUUU Underline placement

U	U	U	U	Line number of underline
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Note: uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

Parameter – ZZZZ Horizontal retrace count

Z	Z	Z	Z	No. of character counts per HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

Parameter – CC Cursor format

C	C	Cursor format
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underline

2 Start display command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Start display	0	0	1	0	0	0	0	0
No parameters											

Action – SAB 8276 interrupts are enabled, DMA requests begin, video is enabled, interrupt enable and video enable status flags are set.

3 Stop display command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Stop display	0	1	0	0	0	0	0	0
No parameters											

Action – Disables video, interrupts remain enabled. HRTC and VRTC continue to run, video enable status flag is reset, and the "Start display" command must be given to re-enable the display.

4 Load cursor position

	Operation	C$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Load cursor	1	0	0	0	0	0	0	0
Parameters	Write	0	Char. number	(Char. position in row)							
	Write	0	Row number	(Row number)							

Action – The SAB 8276 is conditioned to place, the next two parameter bytes into the cursor position registers. Status flags not affected.

5 Enable interrupt command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Enable interrupt	1	0	1	0	0	0	0	0
No parameters											

Action – The interrupt enable status flag is set and interrupts are enabled.

6 Disable interrupt command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Disable interrupt	1	1	0	0	0	0	0	0
No parameters											

Action – Interrupts are disabled and the interrupt enable status flag is reset.

7 Preset counters command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Preset counters	1	1	1	0	0	0	0	0
No parameters											

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU. After this command, two additional clock cycles are required before the first character of the first row is put out.

Status flags

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Read	1	Status word	0	IE	IR	X	IC	VE	BU	X

IE – (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command reset with the "Reset" command.

IR – (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

IC – (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE – (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

BU – (Buffer Underrun) This flag is set whenever a Row Buffer is not filled with character data in time for buffer swap required by the display. Upon activation of this bit, buffer loading ceases, and the screen is blanked until after the vertical retrace interval.

Absolute Maximum Ratings [1]

Temperature under bias	0 to +70 °C
Storage temperature	−65 to +150 °C
All output and supply voltages	−0.5 to +7 V
All input voltages	−0.5 to +5.5 V
Power dissipation	1.0 W

DC Characteristics

(TA = 0 to 70°C, VCC = 5 V ±5%)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC+0.5V	V	–
VOL	Output low voltage	–	0.45	V	IOL = 2.2 mA
VOH	Output high voltage	2.4	–	V	IOH = −400 µA
IIL	Input load current	–	±10	µA	VIN = VCC to 0 V
IOFL	Output float leakage	–	±10	µA	VOUT = VCC to 0.45 V
ICC	VCC supply current	–	160	mA	–

Capacitance

(TA = 25°C, VCC = GND = 0 V)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
CIN	Input capacitance	–	10	pF	fc = 1 MHz
CI/O	I/O capacitance	–	20	pF	Unmeasured pins returned to GND

1) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics (SAB 8276)

(TA = 0 to 70°C, VCC = 5.0 V ± 5%, GND = 0 V)

Clock timing

Symbol	Parameter	Limit values		Units	Test condition
		min.	max.		
TCLK	Clock period	480	–	ns	–
TKH	Clock high	240	–	ns	–
TKL	Clock low	160	–	ns	–
TKR	Clock rise	5	30	ns	–
TKF	Clock fall	5	30	ns	–

Bus parameters
Read cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TAR	Address stable before READ	0	–	ns	–
TRA	Address hold time for READ	0	–	ns	–
TRR	READ pulse width	250	–	ns	–
TRD	Data delay from READ	–	200	ns	CL = 150 pF
TDF	READ to data floating	–	100	ns	CL = 150 pF

Write cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TAW	Address stable before WRITE	0	–	ns	–
TWA	Address hold time for WRITE	0	–	ns	–
TWW	WRITE pulse width	250	–	ns	–
TDW	Data setting time for WRITE	150	–	ns	–
TWD	Data hold time for WRITE	0	–	ns	–

Other timings

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCC	Character code output delay	–	150	ns	CL = 50 pF
THR	Horizontal retrace output delay	–	200	ns	CL = 50 pF
TLC	Line count output delay	–	400	ns	CL = 50 pF
TAT	Control-attribute output delay	–	275	ns	CL = 50 pF
TVR	Vertical retrace output delay	–	275	ns	CL = 50 pF
TRI	INT↓ from RD↑	–	250	ns	CL = 50 pF
TWQ	BRDY↑ from WR↑	–	250	ns	CL = 50 pF
TRQ	BRDY↓ from WR↓	–	200	ns	CL = 50 pF
TLR	$\overline{BS}$↓ to WR↓	0	–	ns	–
TRL	WR↑ to $\overline{BS}$↑	0	–	ns	–

AC Characteristics (SAB 8276-2)

(TA = 0 C to 70°C, VCC = 5.0 V ± 5%, GND = 0 V)

Clock timing

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLK	Clock period	320	–	ns	–
TKH	Clock high	120	–	ns	–
TKL	Clock low	120	–	ns	–
TKR	Clock rise	5	30	ns	–
TKF	Clock fall	5	30	ns	–

Bus parameters
Read cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TAR	Address stable before READ	0	–	ns	–
TRA	Address hold time for READ	0	–	ns	–
TRR	READ pulse width	250	–	ns	–
TRD	Data delay from READ	–	200	ns	CL = 150 pF
TDF	READ to data floating	–	100	ns	CL = 150 pF

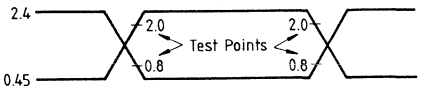
Write cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TAW	Address stable before WRITE	0	–	ns	–
TWA	Address hold time for WRITE	0	–	ns	–
TWW	WRITE pulse width	250	–	ns	–
TDW	Data setting time for WRITE	150	–	ns	–
TWD	Data hold time for WRITE	0	–	ns	–

Other timings

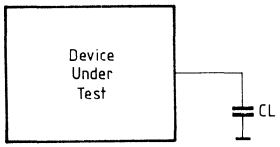
Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCC	Character code output delay	–	150	ns	CL = 50 pF
THR	Horizontal retrace output delay	–	150	ns	CL = 50 pF
TLC	Line count output delay	–	250	ns	CL = 50 pF
TAT	Control-attribute output delay	–	250	ns	CL = 50 pF
TVR	Vertical retrace output delay	–	250	ns	CL = 50 pF
TRI	INT↓ from RD↑	–	250	ns	CL = 50 pF
TWQ	BRDY↑ from WR↑	–	250	ns	CL = 50 pF
TRQ	BRDY↓ from WR↓	–	200	ns	CL = 50 pF
TLR	$\overline{BS}$↑ to WR↓	0	–	ns	–
TRL	WR↑ to $\overline{BS}$↑	0	–	ns	–

A.C. Testing input/output



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

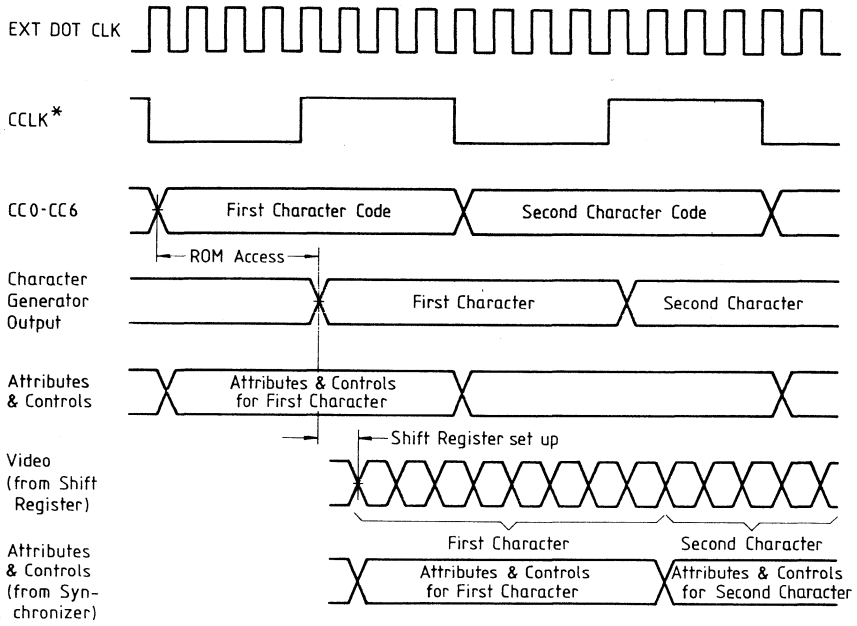
A.C. Testing load circuit



CL Includes Jig Capacitance

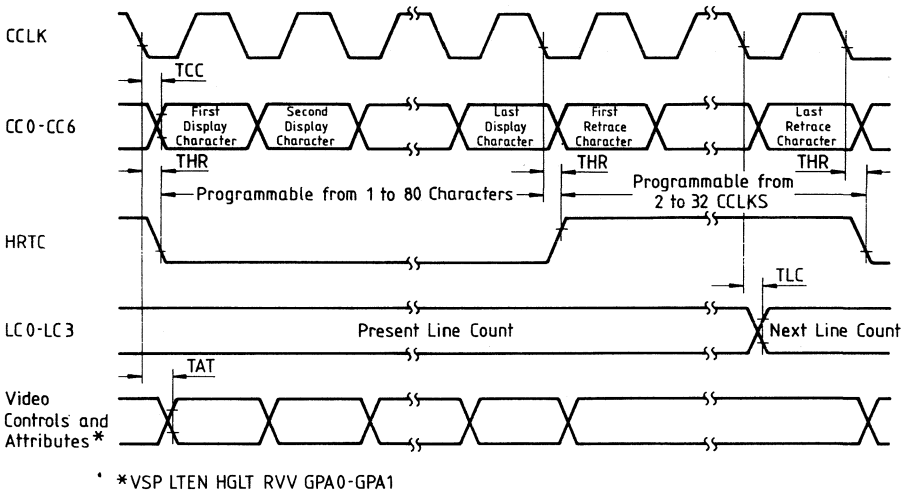
Waveforms

Typical dot level timing

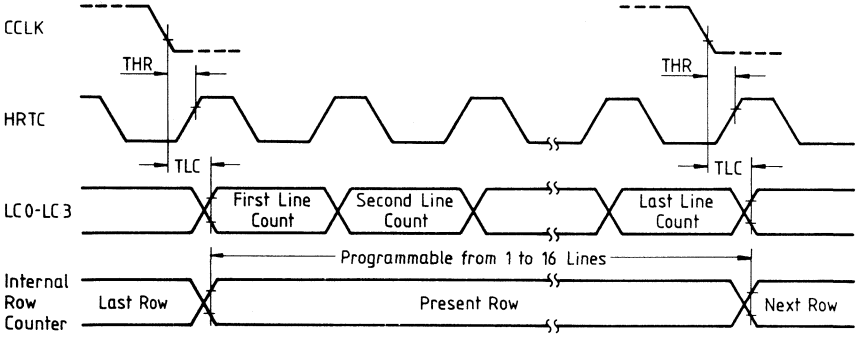


*CCLK is a Multiple of the Dot Clock and an Input to the SAB 8276

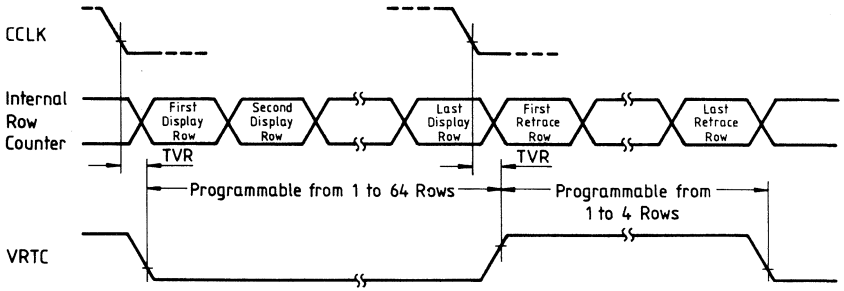
Line timing


CCLK
TCC
CC0-CC6
First Display Character
Second Display Character
Last Display Character
First Retrace Character
Last Retrace Character
THR
THR
THR
Programmable from 1 to 80 Characters
Programmable from 2 to 32 CCLKS
HRTC
TLC
LC0-LC3
Present Line Count
Next Line Count
TAT
Video Controls and Attributes*
*VSP LTEN HGLT RVV GPA0-GPA1

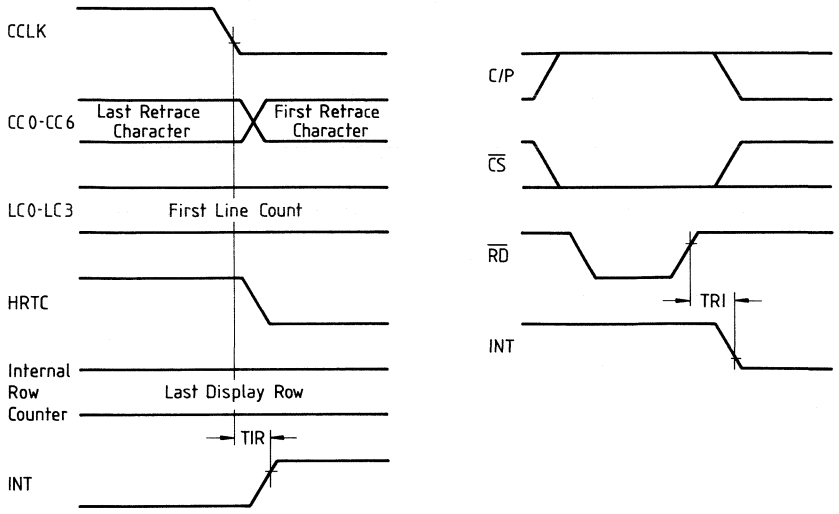
Row timing



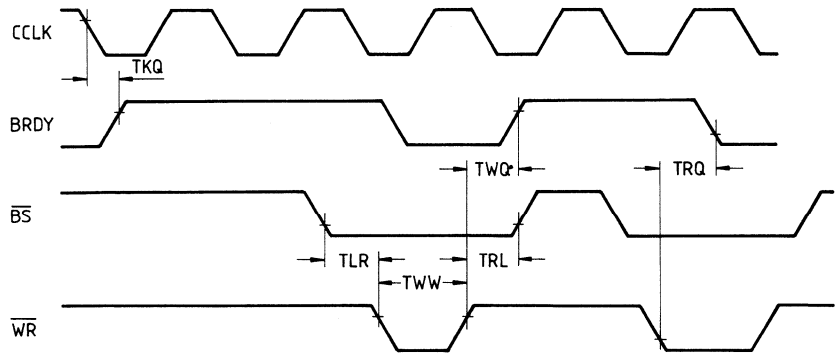
Frame timing



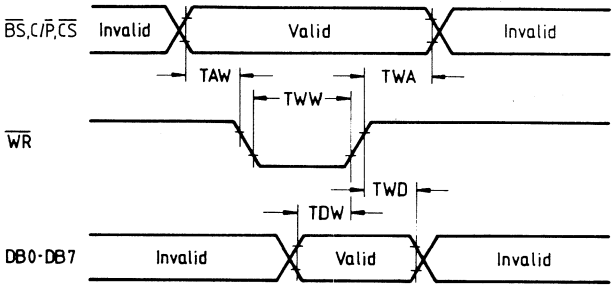
Interrupt timing



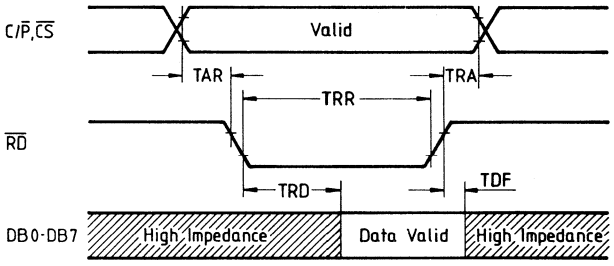
Timing for Buffer Loading



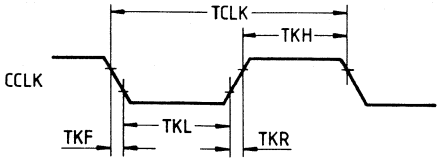
Write timing



Read timing

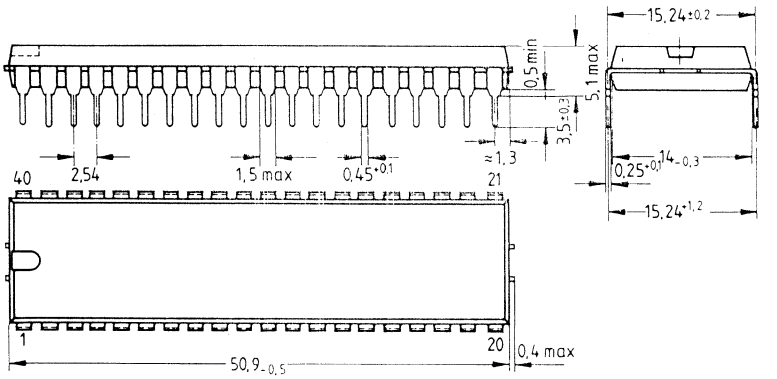


Clock timing



Package outline

Plastic package, P-DIP, 40 pins



Ordering Information

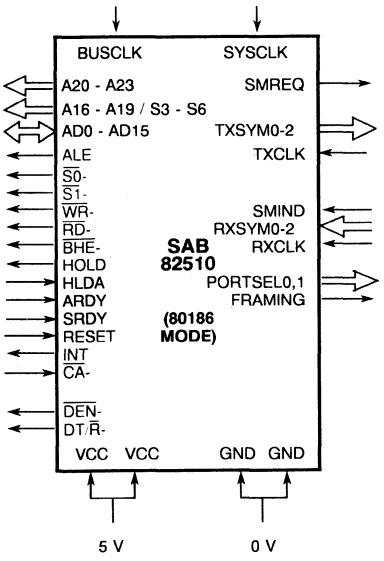
Type	Ordering code	Function
SAB 8276-P	Q67120-P83	Small System CRT Controller, 2 MHz
SAB 8276-2-P	Q67120-P93	Small System CRT Controller, 3 MHz

Advance Information

SAB 82510
Token Bus Controller

- Fully implements the IEEE 802.4 Token Bus Medium Access Sublayer specifications without CPU overhead
- Bus Interface optimized for SAB 80186 and 68000 Bus
- Advanced CMOS
- Up to 10 Mbit/s Serial Data Transfer Rate
- On-Chip DMA Controller
- On-Chip Command and Data Chaining
- Two addressing modes: Segmented or 24 bit physical address
- Four Levels of Priority for Receive and Transmit
- Request with Response including Data Response
- On-chip real time clock support
- 68-pin PLCC package

Logic Symbol



Pin Names

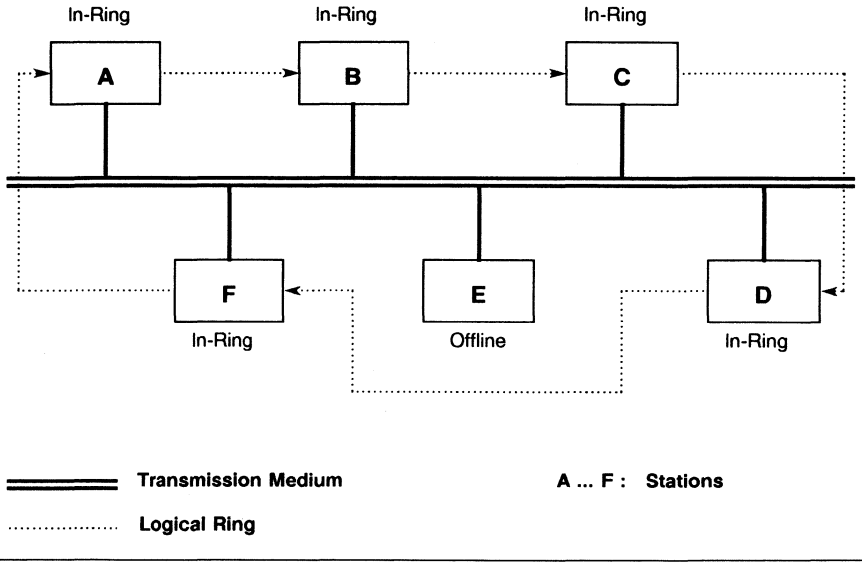
AD0-AD15	Address/Data Bus
A16/S3-A19/S6	Address Bus/Status Lines
A20-A23	High order Address bits
$\overline{S0}$, $\overline{S1}$	Status Lines
ALE	Address Latch Enable
$\overline{WR}$	Write Strobe
$\overline{RD}$	Read Strobe
$\overline{BHE}$	Byte High Enable
HOLD	Hold Request
HLDA	Hold Acknowledge
ARDY	Asynchronous Ready
SRDY	Synchronous Ready
RESET	Reset
$\overline{INT}$	Interrupt Request
$\overline{CA}$	Channel Attention
$\overline{DEN}$	Data Enable
DT/$\overline{R}$	Data Transmit/Receive
BUSCLK	Bus Clock
SYSCLK	System Clock
SMREQ	Station Management Request
TXSYM0-2	Transmit Symbols
TXCLK	Transmit Clock
SMIND	Station Management Indication
RXSYM0-2	Receive Symbols
RXCLK	Receive Clock
PORTSEL0,1	Port Select 0,1
INT/$\overline{MOT}$	Intel/Motorola Mode Sel.
FRAMING	Framing

The SAB SAB 82510 is a highly integrated Token Bus Controller implemented in +5 V advanced Siemens CMOS technology. It effectively combines several high integrated systems components into one chip. Its software interface is designed for real time applications. Intel and 80186 are trademarks of Intel Corporation, Motorola and 68000 are trademarks of Motorola, INC. 1.88

Basic Token Bus Concept

A local-area network employing a high-speed transmission bus configuration is shown in the following figure. The bus consists of a set of stations connected by a transmission medium bus. Data is transferred bit serially between stations via the bus. Each station contains an adapter through which one or more attached bus users (terminals, computers) communications with other users on the bus. A station transfers data from one of its users to a designated destination station using the bus as the link.

Token Bus Example



On a token bus, a station gains the right to transmit data when it captures a free token – a control pattern that circulates on the bus between data transfers. A bus station capturing a free token may use the token to transmit a frame if one is pending or pass the token to the next station in the logical ring (Because each station knows its successor and previous address the stations can be considered to be connected in a logical ring).

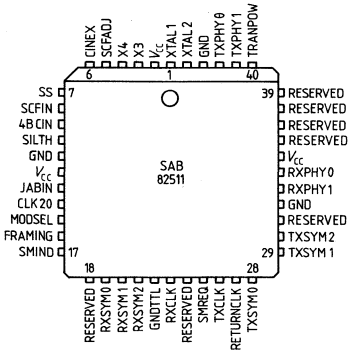
The TBC uses a single token protocol. Only one token circulates on the bus at any time. When a station wants to transmit a message it captures the free token and transforms it to a frame. The TBC may send a single frame per token or multiple frames up to a programmed maximum transmission time limit.

Advance Information

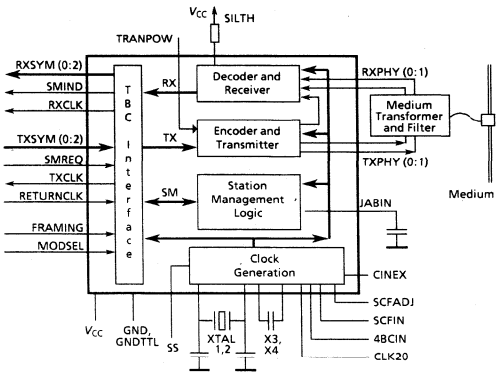
SAB 82511
Token Bus Modem

- Carrier-band modem fully compatible with IEEE 802.4 and MAP Standard
- Interface optimized to SAB 82510 Token Bus Controller
- 5 and 10 Mbit/s data rate using phase-coherent FSK modulation
- Digital PLL and digital demodulation
- Diagnostic loop-back for test purposes
- Provides physical station management
- Jabber inhibit timer (watchdog)
- Differential input/output drivers to serial line
- No active external components
- Advanced Siemens oxid-isolated bipolar technology
- Single +5 V power supply

Pin Configuration



Block Diagram



The token bus modem is designed to work directly with the SAB 82510 token bus controller in IEEE 802.4 token bus applications. It uses phase-coherent frequency shift keying modulation at a data rate of 5 Mbit/s and 10 Mbit/s.
The major functions of the modem are to generate the receive and transmit clock, modulate and demodulate (frequency shift keying) and provide the electrical interface to the transceiver cable.

Diagnostic loop-back control enables the modem to route the signal to be transmitted from the token bus controller through the encoding and decoding circuitry and back to the token bus controller. The combined loop-back capabilities of the token bus controller and the token bus modem result in efficient fault detection. An on-chip failsafe watchdog timer circuit prevents the station from locking up in continuous transmit mode. 10.87

Pin Definitions and Functions

The modem pins are divided into six functional groups:

- Request Channel
- Indication Channel
- Medium Interface
- Operational Mode Selection
- External Clocking
- Power Supply and External Components

All TTL inputs are driven high by internal pullups if not connected.

Request Channel

Symbol	Pin	Input (I) Output (O)	Function
SMREQ	25	I	Selects either MAC mode or station management mode (MAC mode = 1)
TXSYM2 TXSYM1 TXSYM0	30 29 28	I	Encoded MAC symbols for transmission or station management requests
TXCLK	26	O	Transmit clock provided by the modem (5 MHz or 10 MHz)
RETURNCLK	27	I	Transmit clock derived from TXCLK

Indication Channel

Symbol	Pin	Input (I) Output (O)	Function
SMIND	17	O	Indicates either MAC mode or station management mode (MAC mode = 1)
RXSYM2 RXSYM1 RXSYM0	21 20 19	O	Encoded MAC symbols for reception or station management indications and confirmations
RXCLK	23	O	Receive clock provided by the modem (5 MHz or 10 MHz)

Medium Interface

Symbol	Pin	Input (I) Output (O)	Function
RXPHY0 RXPHY1	34 33	I	Differential input lines from the medium transformer
TXPHY0 TXPHY1	42 41	O	Differential output lines to the medium transformer

Operational Mode Selection

Symbol	Pin	Input (I) Output (O)	Function
MODSEL	15	I	Enables modem to react to MAC and station management requests (enable: MODSEL = 1)
SS	7	I	Selects frequency of TXCLK and RXCLK (10 MHz: SS = 1)
FRAMING	16	I	Indicates frame duration. FRAMING is driven high after detection of frame start sequence and driven low after end of frame, frame abort or reset. (Only used for repeaters and redundant media)

External Clocking

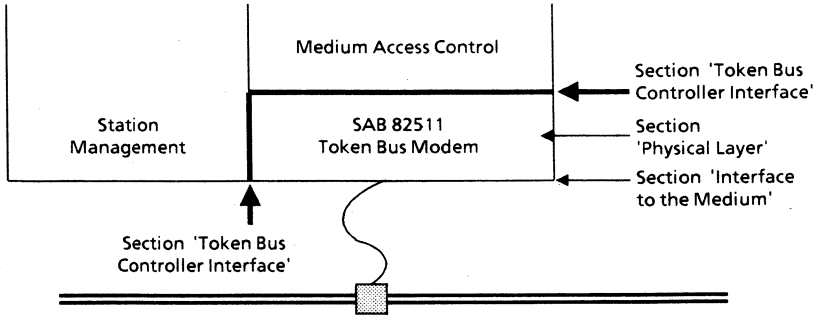
Symbol	Pin	Input (I) Output (O)	Function
CINEX	6	I	Selects internal or external clock generator. If CINEX = high, then external clock must be supplied at SCFIN and 4BCIN. If low, the internal clock generator is used and pins SCFIN and 4BCIN should be left open
SCFADJ	5	I	Adjusts the asynchronous internal clock, if CINEX is low
SCFIN	8	I	External asynchronous clock must be supplied, if CINEX is high. The clock frequency has to be between 16.001 and 16.01 times the bit frequency
CLK20	14	O	20 MHz output of internal clock generator, signal has TTL level
4BCIN	9	I	External clock 4 times bit frequency must be supplied, if CINEX is high (tolerance $\pm$ 0.01%)

Power Supply and External Components

Symbol	Pin	Input (I) Output (O)	Function
SILTH	10	I	Silence threshold. This pin is used to adjust the threshold of silence recognition with a resistor
XTAL1 XTAL2	1 44	I	Connect 20 MHz crystal to use internal clock generator. Instead, an external 20 MHz clock can be AC- coupled to XTAL2
X3 X4	3 4	I	Connect external capacitor for internal clock generator
JABIN	13	I	Connect external capacitor to ground to define JABBER INHIBIT time
TRANPOW	40	I	Adjusts transmitter output level
VCC	2, 12, 35	–	Power supply for digital logic and output drivers
GND	11, 32, 43	–	Circuit ground
GNDTTL	22	–	TTL ground
RESERVED	18, 24, 31, 36, 37, 38, 39	–	These pins are reserved and must be left open. No connections are allowed

Token Bus Controller Interface

Modem Interface to MAC and SMT



The interface (see figure above) provides means for transferring information between modem and medium access control (MAC) and between modem and station management. In the interest of minimizing the number of signal lines, the station management uses the same lines as the MAC to access the modem. The interface supports three primary functions, described below:

Request Channel MAC Mode

The MAC mode is selected when SMREQ = 1 and is considered "normal" operation. The MAC defines 5 symbols for transmission: silence, non-data, one, zero and pad-idle (see next table). The MAC sends these symbols on lines TXSYM0, TXSYM1 and TXSYM2 to the modem. The modem modulates its transmit carrier signal accordingly. These requests are synchronized to RETURNCLK.

MAC request symbol encoding

	SMREQ	TXSYM2	TXSYM1	TXSYM0
Silence	1	1	1	Don't Care
Non-Data	1	1	0	Don't Care
Pad-Idle	1	0	1	Don't Care
One	1	0	0	1
Zero	1	0	0	0

Indication Channel MAC Mode

The MAC mode is indicated by SMIND = 1. The MAC defines 5 symbols for data reception: silence, non-data, bad-signal, one and zero (see next table). The modem reports these symbols on lines RXSYM0 - RXSYM2 to the MAC, synchronized to RXCLK. MODSEL does not affect reception.

MAC indication symbol encoding

	SMIND	RXSYM2	RXSYM1	RXSYM0
Silence	1	1	1	X
Non-Data	1	1	0	X
Bad-Signal	1	0	1	X
One	1	0	0	1
Zero	1	0	0	0

X = either 0 or 1

Physical Layer Management

The request channel and the indication channel serve a second purpose which is to pass station management requests to the modem and to pass station management confirmations and indications to the station management.
Serial commands are not supported.

Management Request

The management mode is selected by SMREQ = 0. The request channel is used by the station management to send station management requests to the modem (for encoding see table below).
The modem must be enabled by MODSEL. All unused commands are not supported.

Note: The transmitter is disabled whenever the modem is in management mode.

Management request encoding

	SMREQ	TXSYM2	TXSYM1	TXSYM0
RESET	0	1	1	1
LOOP-BACK DISABLE	0	1	0	1
ENABLE TRANS-MITTER	0	0	1	1
IDLE/ SERIAL DATA	0	0	0	*

* TXSYM0 contains a start bit, eight data bits and a stop bit, when the MAC issues a SERIAL DATA command. Otherwise, TXSYM0 = 1.

RESET initiates the modem, disables the transmitter and enables the loop-back.

LOOP-BACK DISABLE disables the loop-back at the point closest to the cable between TXPHY and RXPHY.

ENABLE TRANSMITTER switches the transmission path from TXSYM0-TXSYM2 to the differential output lines to the medium.

IDLE indicates that the MAC layer is waiting.

Management Indication/Confirmation

The management mode is indicated by SMIND = 0. The indication channel is used by the modem to send reponses (confirmations) to management commands and to indicate modem fault (PHYSICAL ERROR indication).

The table below shows the encoding for the indication channel management mode. Use of the signal lines is described in the following.

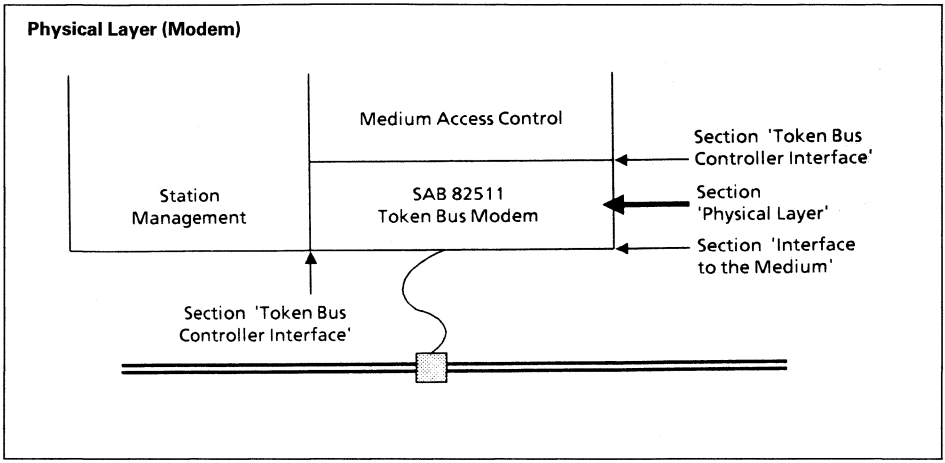
Management indication/confirmation encoding

	SMIND	RXSYM2	RXSYM1	RXSYM0
NAK (non-acknowl-edgement)	0	1	0	*
ACK (acknowl-edgement)	0	0	1	1
IDLE	0	0	0	1
PHYSICAL ERROR	0	1	1	1

* RXSYM0 contains a start bit, "don't care" data and a stop bit, when responding to a serial data command. Otherwise, RXSYM0 = 1.

Management mode (SMIND = 0) is entered in response to SMREQ = 0 as confirmation that the modem has gone to management mode.
Management mode is also entered as a result of a PHYSICAL ERROR condition (indication). For the first case the modem will enter management mode (SMIND = 0) after SMREQ goes low and will leave management mode when SMREQ goes high.
For the second case, the modem will enter management mode and stay until the station management corrects the error and leaves management mode.

Physical Layer



Symbol Encoding

When in MAC mode, the modem transmits symbols received at its MAC interface to the medium. Each of these MAC symbols is encoded into a pair of PHY symbols out of a three-symbol (H), (L), (off) code and then transmitted. The encoding for each of the input MAC symbols is:

(1) **Silence** Each silence symbol is encoded as the sequence (off off).

(2) **Pad-Idle** Successive pad-idle symbols are encoded as an alternating series of (LL) and (HH).

(3) **Zero** Each zero symbol is encoded as the sequence (HH).

(4) **One** Each one symbol is encoded as the sequence (LL).

(5) **Non-Data** Non-Data symbols are transmitted by the MAC in pairs. Each such pair of consecutive non-data symbols is encoded as the sequence (HL, LH).

Line Signal (at the line output of the modem)

The PHY symbols resulting from the symbol encoding are converted directly to their line representation, as described below, and the resulting signaling is ac-coupled to the single channel phase-coherent FSK bus medium. The modem is able to receive signals of either polarity.

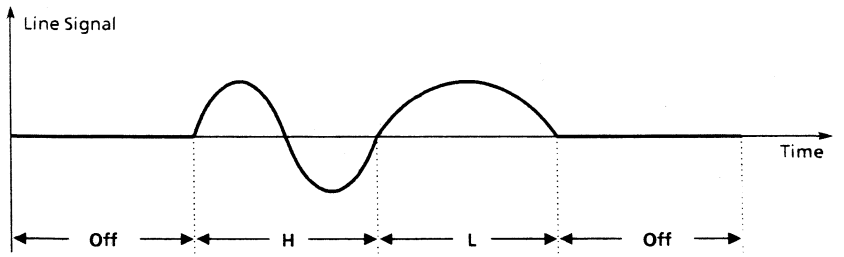
The line signal representations of the (H), (L) and (off) PHY symbols is as follows (see also figure below):

(1) An (H) is represented as one full cycle of a signal starting and ending with a nominal zero amplitude, the period of which is equal to half the period of MAC symbol delivery to the MAC entity at the MAC interface.

(2) An (L) is represented as one half cycle of a signal, starting and ending with a nominal zero amplitude, the period of which is equal to the period of MAC symbol delivery to the MAC entity at the MAC interface, with the phase of the representing half cycle changing at each successive (L).

(3) An (off) is represented by no signal for a period equal to one half of the period of MAC symbol delivery to the MAC entity at the MAC interface.

Symbolic Line Signal Representation

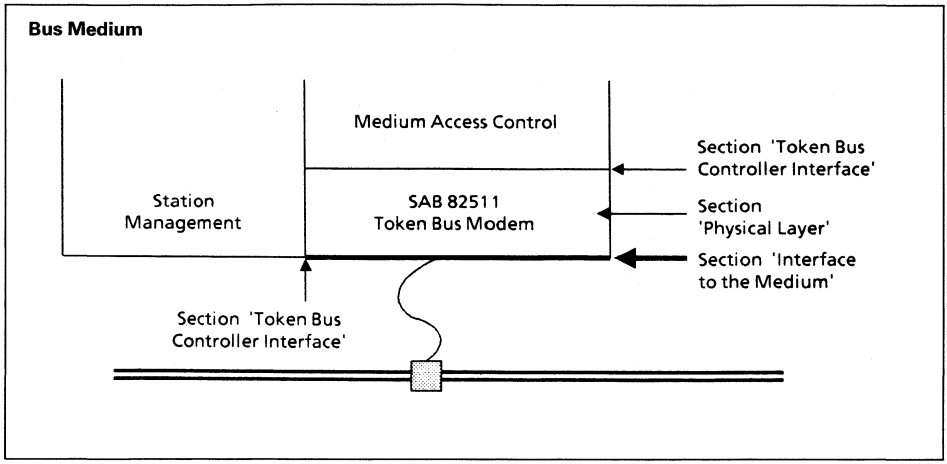


The maximum jitter in the period of any (L) or half-cycle of any (H) is not more than ±1 percent of the MAC symbol period.
The next table summarizes the relationship of data rate and signaling frequencies.

Data Rate vs. Signaling Frequencies

Data Rate (Mbps)	Frequency of Lower Tone (MHz)	Frequency of Higher Tone (MHz)
5	5.0	10.0
10	10.0	20.0

Interface to the Medium



All measurements specified in the following paragraphs are to be made at the point of station or regenerative repeater connection to the medium. Unless otherwise stated, all voltage and power levels specified are in rms and dB (1 mV, 75 ohm) [dBmV] rms, respectively, based on measuring the fundamental signal content of continuous transmissions of all 'one' or all 'zero' symbols.

Coupling to the Medium

The connection of the single-channel phase-coherent FSK bus medium to the station shall be of a flexible 75 ohm drop cable terminated in a male F-series 75 ohm connector; this combination shall mate with a female F-series 75 ohm connector mounted on the station.
In addition to this coupling, the shield(s) of the coaxial drop cable medium shall be connected to the shell of the terminating male connector and the DC impedance of that connection shall be less than 0.1 ohm. Also the DC impedance of a connection between the shell of that male connector and the outer barrel of a mated female connector shall be less than 0.1 ohm.

Characteristic Impedance

The characteristic impedance of the single-channel phase-coherent FSK bus medium shall be 75 ± 3 ohm. The physical medium shall present an impedance to the station resulting in a VSWR of 1.5 : 1 or less when driven from a 75 ohm source over the operating frequency range.

Signal Level

When receiving the signal of a single station or regenerative repeater the single channel phase-coherent FSK bus medium shall present that signaling to the connected station or regenerative repeater at an amplitude between +10 dB and +66 dB (1 mV, 75 ohm) [dBmV] for a 5 Mbit/s data rate and a 10 Mbit/s data rate.
The signal strength of the two fundamental signaling frequencies due to media attenuation (corresponding to the data rate and twice the data rate) at any receiving station shall vary by no more than 3.5 dB.

Note: This is equivalent to the cable tilt found on 500 meters of foam dielectric RG-11 type cable with 8.2 dB of attenuation at 10 MHz.

Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
All output and supply voltages	−0.5 to V_{cc} +0.5V
All input voltages	−0.5 to +5.5V
Power dissipation	1.55W

DC Characteristics for TTL Voltages

T_A = 0 to 70 °C; V_{CC} = +5V ± 5%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	–	0.8	V	–
V_{IH}	Input high voltage	2.0	–	V	–
V_{OL}	Output low voltage	–	0.5	V	at 8mA
V_{OH}	Output high voltage	2.5	–	V	at −1.0mA
V_C	Input clamp voltage	−1.0	–	V	I_C = −5mA
I_{IL}	Input low current	–	−2.0	mA	at V_{IL} =0.5V
I_{IH}	Input high current	–	50	μA	at V_{IH} = 2.7V
I_{CC}	Power supply current	–	290	mA	T_A = 25°C all outputs open signal levels 0.5V/3.5V
I_L	Input leakage current	–	–	μA	V_R = 5.25V
I_{OFF}	Output off current	–	20	μA	0.45V< V_{OFF}< 5.25V
C_{IN}	Input capacitance	–	10	pF	f = 1MHz V_{CC} = 5V T_A = 25°C V_{BIAS} = 2.5V

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ±5%

Token Bus Controller Interface (10 Mbit/s)

Symbol	Parameter	Limit values			Unit
		min.	typ.	max.	
60a	RXCLK period	90	100	110	ns
60b	TXCLK period	90	100	110	ns
61	RXCLK sum of 3 periods	270	300	330	ns
62	RXCLK/TXCLK low time	40	50	60	ns
63	RXCLK/TXCLK high time	40	50	60	ns
64	RXCLK/TXCLK rise/fall time	–	–	10	ns
65	RETURNCLK/TXSYM/SMREQ setup time	35	–	–	ns
66	RETURNCLK/TXSYM/SMREQ hold time	10	–	–	ns
67	RXCLK/RXSYM/SMIND setup time	40	–	–	ns
68	RXCLK/RXSYM/SMIND hold time	10	–	–	ns
60	RXCLK period when reporting silence or pad idle	90	–	210	ns
61	RXCLK sum of 3 periods during synchronization	270	–	430	ns
62	RXCLK low time during synchronization	40	–	170	ns
63	RXCLK high time during synchronization	40	–	170	ns

Token Bus Controller Interface (5 Mbit/s)

Symbol	Parameter	Limit values			Unit
		min.	typ.	max.	
60a	RXCLK period	180	200	220	ns
60b	TXCLK period	180	200	220	ns
61	RXCLK sum of 3 periods	540	600	660	ns
62	RXCLK/TXCLK low time	80	100	120	ns
63	RXCLK/TXCLK high time	80	100	120	ns
64	RXCLK/TXCLK rise/fall time	–	–	10	ns
65	RETURNCLK/TXSYM/SMREQ setup time	70	–	–	ns
66	RETURNCLK/TXSYM/SMREQ hold time	10	–	–	ns
67	RXCLK/RXSYM/SMIND setup time	80	–	–	ns
68	RXCLK/RXSYM/SMIND hold time	10	–	–	ns
60	RXCLK period when reporting silence or pad idle	180	–	420	ns
61	RXCLK sum of 3 periods during synchronization	540	–	860	ns
62	RXCLK low time during synchronization	80	–	340	ns
63	RXCLK high time during synchronization	80	–	340	ns

Receiver Characteristics

Symbol	Parameter	Limit values			Unit
		min.	typ.	max.	
V_I	Input voltage at RXPHY0 and RXPHY1	GND	–	V_{CC}	–
P_I	Input power for normal receive operation	10	–	66	dBmV
C_I	Input capacitance	*	*	*	–
L_I	Input impedance	1	–	–	kΩ
SNR	Signal/noise ratio for normal receive operation	–	20	–	dB
BER	Bit error rate for normal receive operation	–	–	10E-9	–

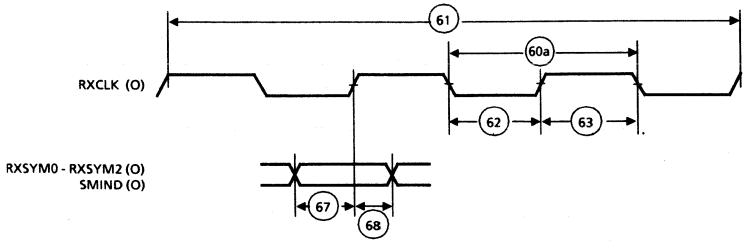
Transceiver Characteristics

Symbol	Parameter	Limit values			Unit
		min.	typ.	max.	
V	Voltage at TXPHY0 and TXPHY1	*	–	*	–
I_O	Output current for transmit operation	*	–	*	–
P_O	Output power for transmit operation	63	–	66	dBmV
t_r	Output current rise time	*	–	*	–
t_f	Output current fall time	*	–	*	–

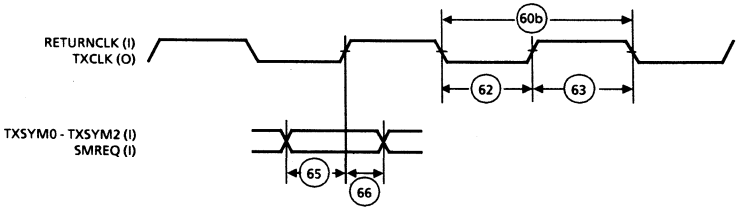
* = to be defined

Waveforms

Receive Timing

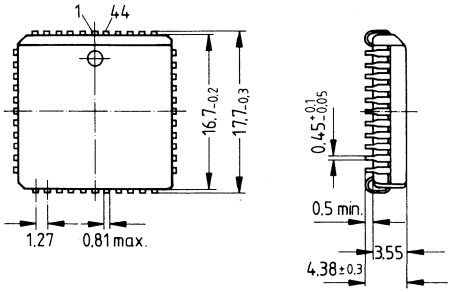


Transmit Timing



Package Outlines

Plastic Package (chip-carrier)
PL-CC-44 (SMD)



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 82511-N	Q67020-P-51	Token bus modem

HSCC
High-Level
Serial Communications Controller
SAB 82520
SAF 82520

Preliminary Data **CMOS IC**

Features

- Two independent HDLC channels
- Implementation of X.25 LAPB/LAPD protocol
- Programmable timeout and retry conditions
- FIFO buffers for efficient transfer of data packets
- Digital phase-locked loop for each channel
- Baudrate generator and oscillator
- Different modes for clock recovery and data encoding
- High-speed data rate (up to 4 MHz)
- Supports bus configuration by collision resolution
- Telecom-specific features programmable
- 8-bit parallel µP interface
- Advanced CMOS technology
- Low power consumption; active: 25 mW at 4 MHz
  standby: 3 mW
- Package: P-DIP-28, C-DIP-28 or PL-CC-28
- SAB 82520: operating temperature 0 to 70 °C
- SAF 82520: operating temperature –40 to 85 °C

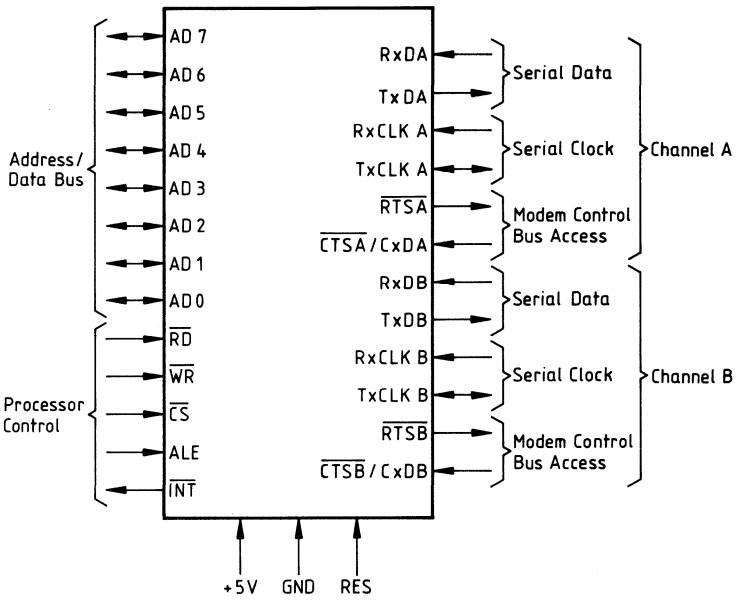
General Description

SAB 82520, a high-level serial communications controller (HSCC), has been designed to free the user from tasks occuring in communication via networks and trunk lines.

SAB 82520 is an X.25 LAPB/LAPD controller which, to a large degree performs communication procedures independently of CPU support.

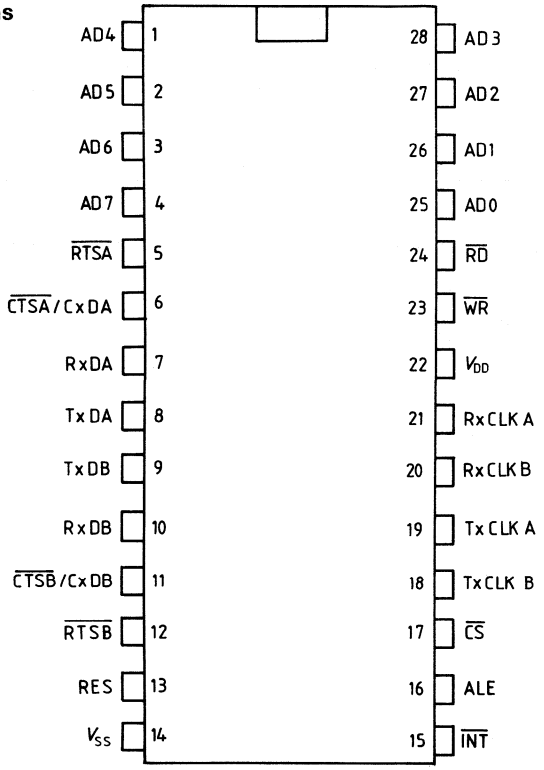
A parallel processor bus constitutes the µC system. The communications interface is implemented by two full-duplex HDLC channels, which can be operated independently from one another. The HSCC is connected to the transmission line via additional line drivers or modems. External logic is cost-effective because clock recovery can be performed by an on-chip oscillator, DPLL circuits and a programmable baudrate generator.

Logic Symbol

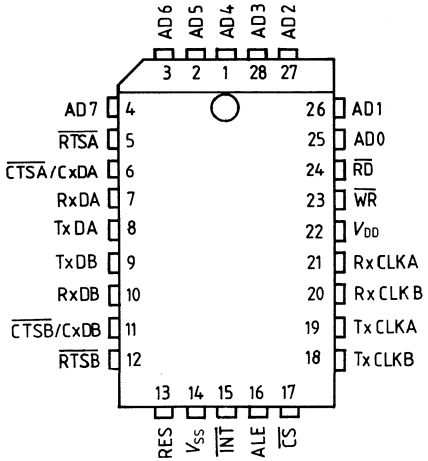


Pin configurations
(top view)

P-DIP-28
C-DIP-28



PL-CC-28



Applications

Point-to-Point Configuration

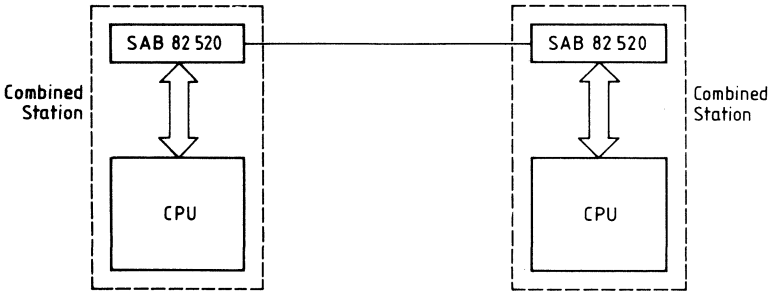


Figure 1a

Point-to-Multipoint Configuration

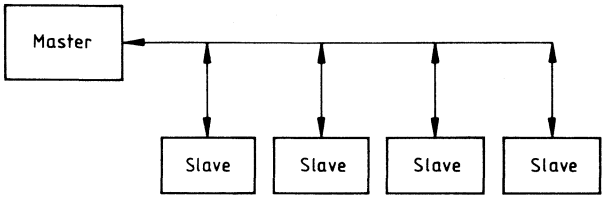


Figure 1b

Multimaster Configuration

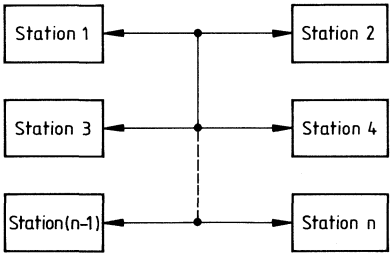


Figure 1c

In a point-to-multipoint or in a multimaster configuration the HSCC can be used as a central station (master) or a peripheral station. As a peripheral station the HSCC can initiate the transmission of data. An internal function block provides for collision avoidance, which may occur if several stations start the transmitting simultaneously.

Furthermore, in a special operating mode the HSCC can transmit or receive data packets in programmable time slots; this makes SAB 82520 especially suitable for applications in systems designed for packet switching. In this application in particular, the integrated collision-resolution mechanism provides optimal utilization of system-internal PCM paths.

Characteristics

A number of characteristics which distinguish the SAB 82520 from conventional low-level HDLC devices are described below.

Support of Layer-2 Functions by HSCC

"Low-level" HDLC devices usually support various of protocols. When applying the HDLC protocol mainly bit-oriented functions such as bit stuffing, CRC check, flag and address recognition are performed. SAB 82520 has been especially designed to support the ISO HDLC protocol. In addition to the bit-oriented functions, the device provides a high degree of procedural support and evaluates the layer-2 control field. The communications procedures are processed between the communications controllers and not between the processors. As a result procedure handshaking is no longer necessary. The processor is informed of the status of the procedure however. The dynamic load of the processor is thus largely reduced. To maintain cost effectiveness and flexibility, not all layer 2 functions have been implemented as hardware. Instead, functions such as connection setup/connection cleardown and error recovery in case of protocol errors are performed by the processor software.

Operating Modes

The distribution of functions between HSCC and CPU applies to the auto mode. As a prerequisite for this operating mode, the window size between transmitted and acknowledged frames has to be limited to 1. Alternatively, transparent modes can be applied, the data field as well as the layer-2 headers are forwarded directly to the CPU. The reception and transmission of messages is fully controlled by the CPU. This operating mode is selected when the component is used as a central station (master) or if the accepted distance between transmitted and received frames (window size) is larger than 1.

Furthermore, there is a possibility to bypass the receiver and to get access to the received data directly.

FIFO Buffers for Efficient Transfer of Data Packets

Another feature of the SAB 82520 can be seen in the buffers that are used for temporary storage of data packets which are transferred between the serial communication interface and the parallel system bus. Due to the overlapping input/output operation (dual-port

behavior), the maximum length of the data packets is not limited by the buffer size . The dynamic load of the processor is reduced by transferring the data packets block by block.

One FIFO buffer with a total capacity of 64 bytes per direction and channel is divided into two memory pools of 32 bytes each. When a pool is filled (receive mode) or emptied (transmit mode) via the serial interface, the processor is prompted by interrupt to read or write this pool. Subsequently the second pool is filled or emptied. During this time the CPU can transfer the first block thereby ensuring availability of the pool. With a serial transfer rate of 1 Mbit/s the reaction time between the first promting and data overflow with loss of data is 256 µs. In addition, the transmit FIFO provides the flexibility for temporarily storing blocks of various lengths, which can be received in rapid succession. The FIFO will also store a data packet when a preceding short data packet stored in the memory has not yet been read by the processor.

The HSCC is especially suitable for cost-critical applications with single-chip processors due to its memory organization and on-chip memory control.

Move string commands are available for high-performance applications where fast data rates at the communication interface and a high level of processor performance are required. The FIFO can then be addressed by the automatically incremented address.

Serial Interface

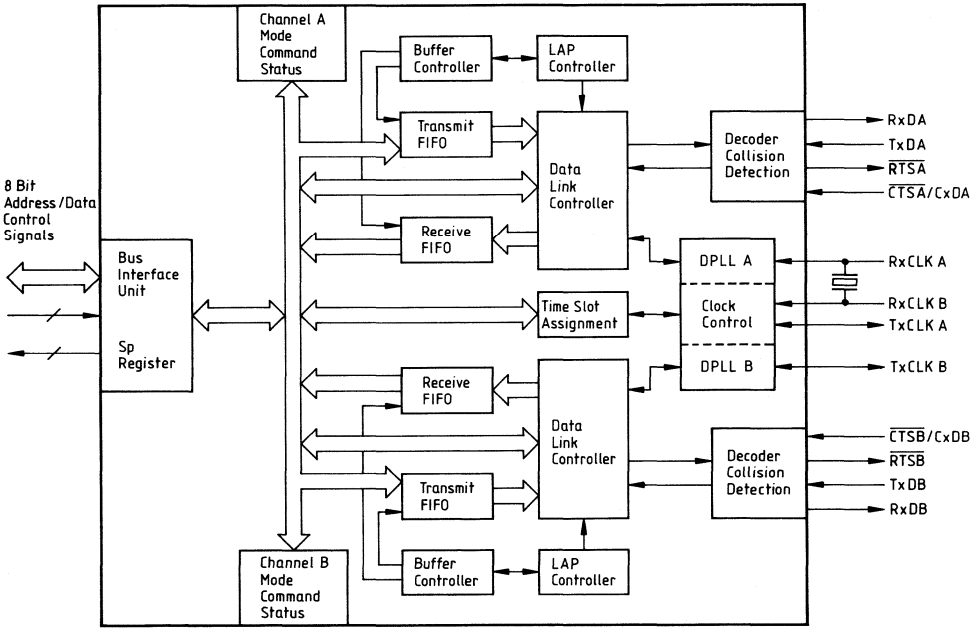
The serial interface provides two independent, high-performance communication interfaces. As already mentioned, the ISO HDLC layer-2 protocol is supported by the HSCC. In addition, layer-1 functions are provided by means of on-chip circuits. Eight different operating modes can be selected to clock the serial data stream.

- During the self-clocked operating mode, the transfer clock is recovered from the received data stream by means of an external crystal only. On-chip oscillator and DPLL circuits sample the received bit stream and adjust the clock edge to the center of the data bit.
- The bit stream is synchronized in the externally clocked operation mode by external clock signals. One the whole, 4 different clock signals separated by direction and channel, can be forwarded.
  In addition to the data clock, an externally supplied strobe signal can be applied to determine the time period during which data is to be received or transmitted. Using another operating mode, a time slot (up to 64 bit) can be programmed for transmitting data and another time slot for receiving data. One time slot consists of eight clock cycles.
- With the point-to-multipoint configuration, comprising a central station (master) and several peripheral stations (slaves), data transmission can be initiated by a slave. If several stations (slaves) transmit data simultaneously, the bus is assigned to one station by a collision-resolution procedure implemented by the HSCC. The bus assignment functions in accordance with the principle applied with the ISDN S bus. Its collision-resolution procedure helps to ensure a sharing of priority among the slave stations.
- The maximum data rate of the externally clocked operating mode is 4 Mbits per second. In the self-clocked operating mode with an external reference clock or the crystal oscillator, the maximum clock rate is 12 MHz, the maximum data rate will be 750 Kbit/ s.

Description of Block Diagram

The chip contains a serial interface for two channels, including a DPLL and collision-detection block, a data-link controller and the FIFO buffers. The µP interface, including the status and command registers, is used for both channels. These functions are implemented in 2µm CMOS technology.

Block Diagram



Pin Definitions and Functions

Pin	Symbol	Input (I) Output (O)	Functions
25 26 27 28 1 2 3 4	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	ADDRESS DATA BUS The multiplexed address data bus transfers data and commands between the µP system and the HSCC
5 12	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O O	$\overline{\text{REQUEST TO SEND}}$ When the RTS bit in MODE is set, the $\overline{\text{RTS}}$ signal goes low. When the RTS bit is reset, the signal goes high if the transmitter has finished and there is no further request for a transmission. In a bus configuration, $\overline{\text{RTS}}$ goes low during the actual transmission of a frame shifted by a clock period, excluding collision bits.
6 11	$\overline{\text{CTSA}}$/C x DA $\overline{\text{CTSB}}$/C x DB	I I	$\overline{\text{CLEAR TO SEND}}$/COLLISION DATA A low on the inputs enables the respective transmitter. If the transmitters are always enabled, $\overline{\text{CTS}}$ should be connected to V_{SS}. In a bus configuration the external serial bus must be connected to the respective C x D pin.
7 10	R x DA R x DB	I I	RECEIVE DATA These lines receive serial data at standard TTL or CMOS levels.
8 9	T x DA T x DB	O O	TRANSMIT DATA These lines transmit serial data at standard TTL or CMOS levels. They can be programmed as push-pull or open-drain outputs.
13	RES	I	RESET A high on this input forces the HSCC into reset state. The HSCC is in power-up mode during reset and in power-down mode after reset. The minimum pulse length is 1.8 µs.
14	V_{SS}		GROUND (0 V)
15	$\overline{\text{INT}}$	O	$\overline{\text{INTERRUPT REQUEST}}$ The signal is activated when the HSCC requests an interrupt. It is an open-drain output.
16	ALE	I	ADDRESS LATCH ENABLE A high on this line indicates an address on the external address data bus, selecting one of the HSCC internal sources or destinations.

Pin Definitions and Functions

Pin	Symbol	Input (I) Output (O)	Functions
17	$\overline{CS}$	I	$\overline{CHIP\ SELECT}$ A low on this signal selects the HSCC for a read/write operation.
18 19	T x CLKB T x CLKA	I/O I/O	TRANSMIT CLOCK These pins can be programmed in several different modes of operation. T x CLK may supply the transmit clock for the respective channel, a receive strobe signal (T x CLKA) and a transmit strobe signal (TxCLKB) or a frame synchronization signal (T x CLKA, clock mode 5). Programmed as outputs, T x CLK supply the transmit clock of the respective channel or a tristate control signal, indicating the programmed transmit time slot (T x CLKB, clock mode 5).
20 21	R x CLKB R x CLKA	I I	RECEIVE CLOCK These pins can be programmed in several different modes of operation. In each channel R x CK may supply the receive clock, the receive and transmit clock, the clock for the baud rate generator or the clock for the DPLL. They also can be programmed for use as a crystal oscillator.
22	V_{DD}		POWER +5 V power supply.
23	$\overline{WR}$	I	$\overline{WRITE}$ This signal indicates a write operation.
24	$\overline{RD}$	I	$\overline{READ}$ This signal indicates a read operation.

Maximum Ratings

			min.	max.	Unit
Storage temperature		T_{stg}	–65	125	°C
Operating temperature:	SAB 82520	T_A	0	70	°C
Operating temperature:	SAF 82520	T_A	–40	85	°C
Voltage at any pin vs. ground		V	–0.4	V_{CC} + 0.4	V

DC Characteristics

SAB 82520: T_A = 0 to 70 °C; V_{CC} = 5 V ±10%; GND = 0 V
SAF 82520: T_A = –40 to 85 °C; V_{CC} = 5 V ±5%; GND = 0 V

		Test conditions	min.	typ.	max.	Unit
L input voltage	V_{IL}		V_{SS} –0.4		0.8	V
H input voltage	V_{IH}				V_{CC} +0.4	V
L output voltage	V_{OL}	I_{OL} = +2 mA			0.45	V
H output voltage	V_{OH}	I_{OH} = –400 µA	2.4			V
		I_{OH} = –100 µA	V_{CC} –0.5	V_{CC}		V
Input leakage current	I_{IL}	V_{IN} = V_{CC} to 0 V	–10		10	µA
Output leakage current	I_{OL}	V_{OUT} = V_{CC} to 0 V	–10		10	µA
V_{CC} supply current						
p. d.	I_{CC}			0.5		mA
p. u.	I_{CC}	V_{CC} = 5 V, CP = 4 MHz Inputs at V_{SS}/V_{CC} No output loads		5	7	mA

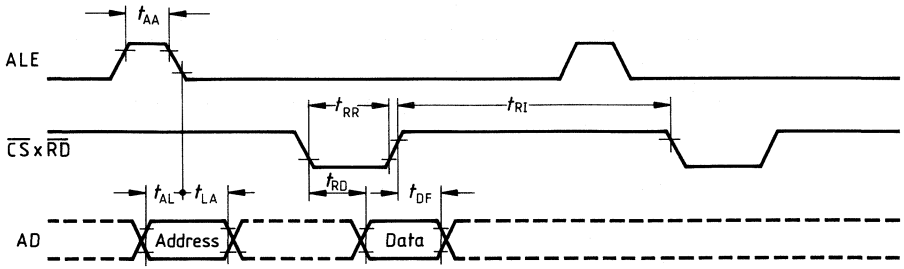
Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

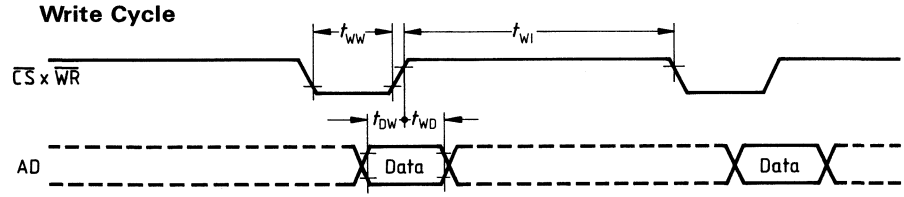
		Test conditions	min.	typ.	max.	Unit
Input capacitance	C_{IN}	f_c = 1 MHz		5	10	pF
Input/output capacitance	$C_{I/O}$			10	20	pF
Output capacitance	C_{OUT}	unmeasured pins returned to GND		8	15	pF

µP Interface Timing

Read Cycle



Write Cycle



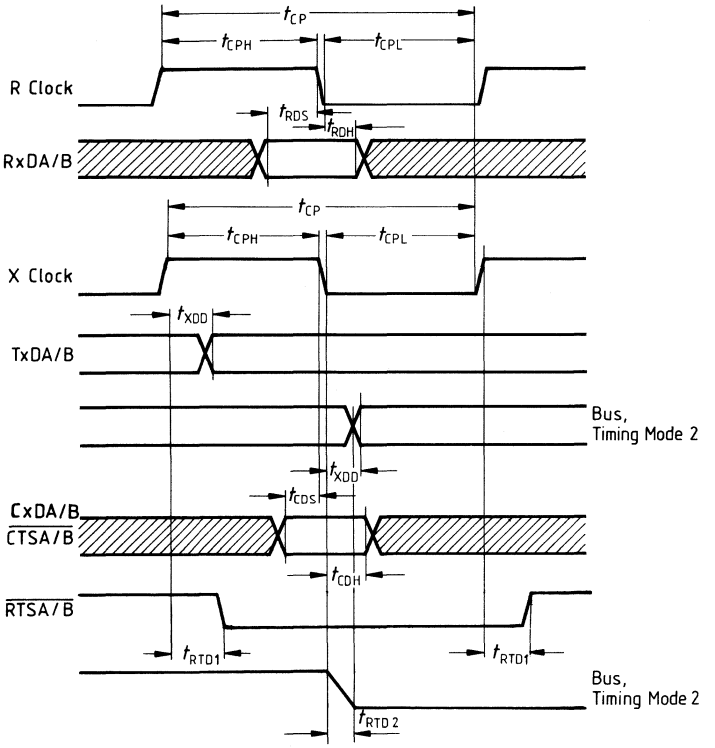
Read Cycle

		min.	max.	Unit
Address hold after ALE	t_{LA}	25		ns
Address to ALE setup	t_{AL}	20		ns
Data delay from $\overline{RD}$	t_{RD}		110	ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	60		ns
ALE pulse width	t_{AA}	50		ns

Write Cycle

		min.	max.	Unit
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup to $\overline{WR}$	t_{DW}	30		ns
Data hold after $\overline{WR}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	60		ns

Serial Interface Timing

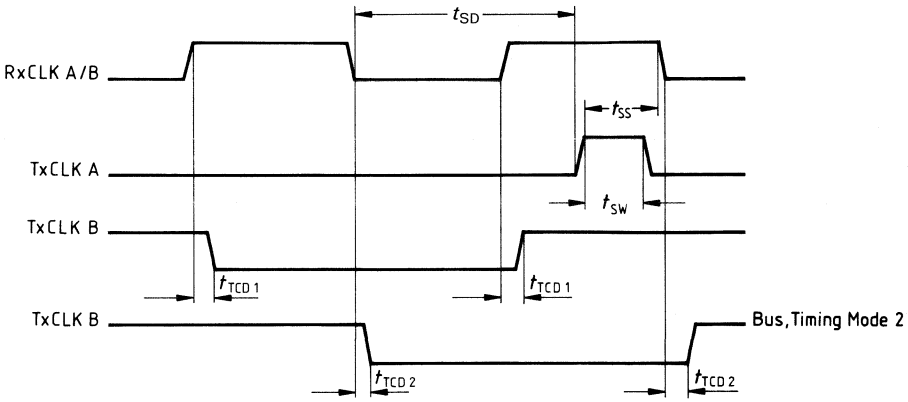


AC Characteristics

SAB 82520: T_A = 0 to 70 °C; V_{CC} = 5 V ±10%; GND = 0 V
SAF 82520: T_A = –40 to 85 °C; V_{CC} = 5 V ±5%; GND = 0 V

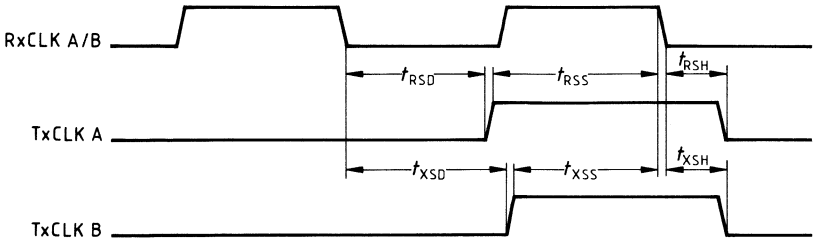
		min.	max.	Unit
Receive data setup	t_{RDS}	0		ns
Receive data hold	t_{RDH}	30		ns
Collision data setup	t_{CDS}	0		ns
Collision data hold	t_{CDH}	30		ns
Transmit data delay	t_{XDD}	20	68	ns
Request to send delay 1	t_{RTD1}	30	120	ns
Request to send delay 2	t_{RTD2}	20	85	ns
Clock period	t_{CP}	240		ns
Clock period Low	t_{CPL}	90		ns
Clock period High	t_{CPH}	100		ns

Clock Mode 5



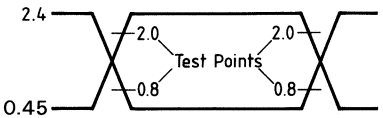
		min.	max.	Unit
Sync pulse delay	t_{SD}	30		ns
Sync pulse setup	t_{SS}	30		ns
Sync pulse width	t_{SW}	40		ns
Time-slot control 2 delay	t_{TCD2}	20	85	ns
Time-slot control 1 delay	t_{TCD1}	30	120	ns

Clock Mode 1

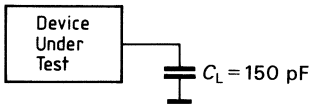


		min.	max.	Unit
Receive strobe delay	t_{RSD}	30		ns
Receive strobe setup	t_{RSS}	70		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe setup	t_{XSS}	70		ns
Transmit strobe hold	t_{XSH}	30		ns

AC Testing Input, Output Waveform



AC Testing Load Circuit



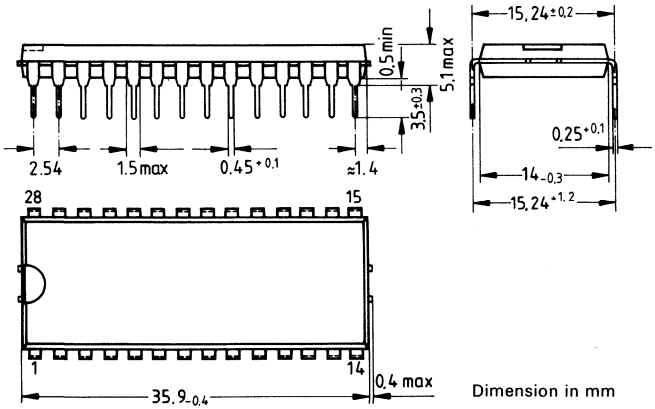
AC Testing

Inputs are driven at 2.4 V for logic "1" and 0.45 V for logic "0".
Timing measurements are made at 2.0 V for logic "1" and at 0.8 V for logic "0".

Ordering Information

Type	Ordering Code	Package
SAB 82520-P	Q67100-H8014	P-DIP-28
SAB 82520-C	Q67100-H8330	C-DIP-28
SAB 82520-W	Q67100-H8400	PL-CC-28 (SMD)
SAF 82520-P	Q67100-H8512	P-DIP-28
SAF 82520-C	Q67100-H8325	C-DIP-28
SAF 82520-W	Q67100-H8610	PL-CC-28 (SMD)

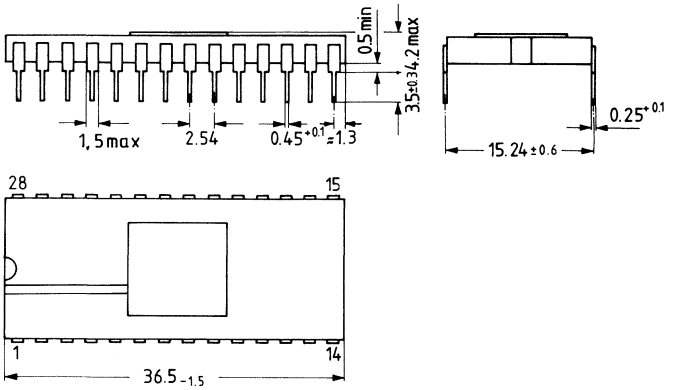
Plastic Package, P-DIP-28
(dual-in-line package)
20 B 28 DIN 41870 T 10



Dimension in mm

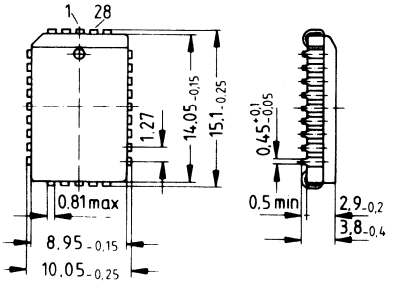
Approx. weight 3 g

Ceramic Package, C-DIP-28
(dual-in-line package)
20 B 28 DIN 41870 T 10



Approx. weight 3.5 g

Plastic Package, PL-CC-28
(Chip carrier)



Dimensions in mm

Surface Mounted Device (SMD)

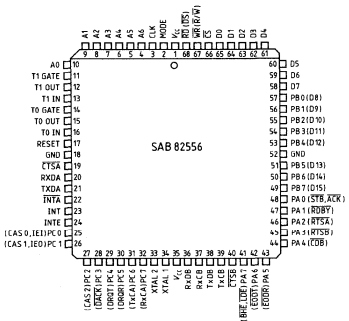
Advance Information

SAB 82556
Universal System Interface Controller

- Flexible Bus Interface direct compatible or easy adaptable to most popular microprocessors (e.g. Intel, Motorola, 1EC NS, Zilog etc.)
- Two multistage buffered serial channels
  - Channel A with asynchronous operation
  - Channel B

  with asynchronous and synchronous operation (e.g. HDLC, SDLC, SDLC loop, Bisgnc, DDCMP ...)
  - 4 byte deep FIFO for transmitter of channel A, 16 byte deep FIFOs for receiver channel A, and transmitter/receiver of channel B
- Enhanced future set of channel B
  - up to 4 Mbit/s transfer rate
  - DMA support
  - Data Encoding on chip
  - Optional 16-bit access to receiver/transmitter FIFOS
  - Support for ISDN and Cheapernet applications
  - Optional interface signals for intelligent DMA controller
- Two Baud Rate Generators on chip with crystal or external clock input
- Three parallel 8-bit input/output ports
  - Each pin individually programmable as input or output
  - Handshake support
- Three 16-bit Timer/Counter (functional subset of SAB 8254)
- Interrupt controller with up to 8 internal and up to 9 external interrupt sources (compatible to SAB 82C59A)
  - Eight priority levels
  - Free assignment of interrupt sources to priority levels
  - Two cascading schemes:
  - SAB 8259A compatible and
  - Daisy Chain cascading scheme.

Pin Configuration



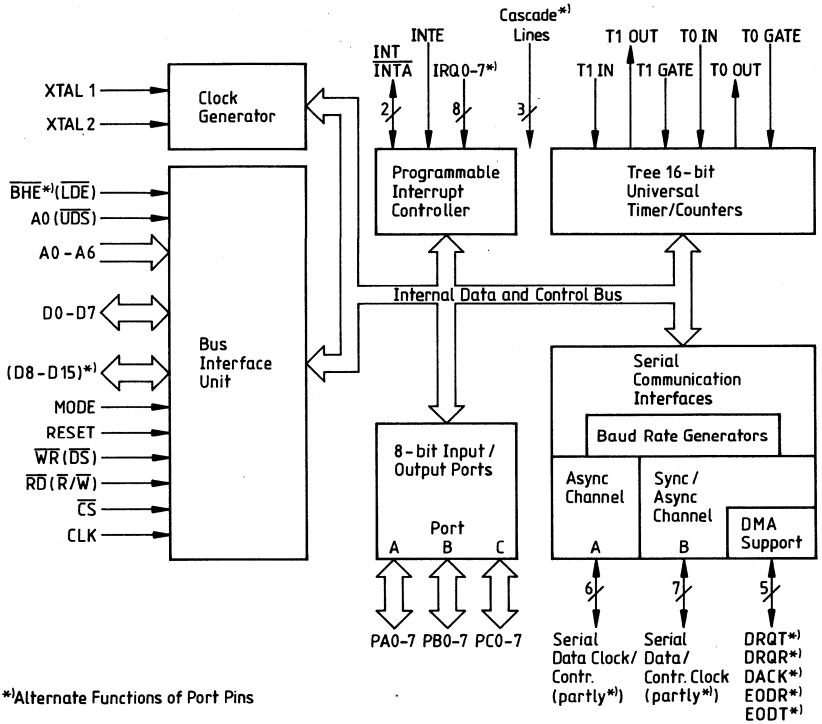
The USIC is a multifunction, multipurpose combo device. It combines system and interface functions normally necessary in every microprocessor system

- Serial Interfaces
- Parallel Interfaces
- Timer/Counters
- Interrupt Controller

together with a flexible, adaptable bus interface. Moreover support functions like clock generator, baudrate generators, DMA-support etc. are integrated into the device. Made with CMOS technology and housed in a 68-pin package the USIC provides a power and board space saving cost effective solution for microprocessor systems.

2.88

Block Diagram



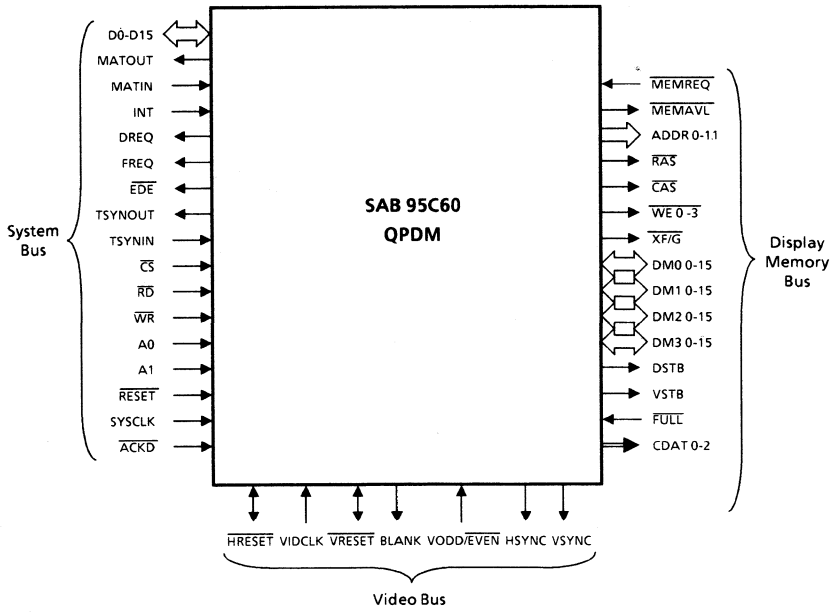
*)Alternate Functions of Port Pins

Advance Information

SAB 95C60
Quad Pixel Dataflow Manager (QPDM)

- Generates mixed text and graphics within display memory
- Draws vectors up to 3.3 million pixels per second, or places text at 45,000 characters per second
- One chip handles four display memory planes of any size up to 4K × 4K bits and screen sizes up to 2K × 2K pixels
- Capable of cascading to handle multiple memory planes without system perfomance degradation
- Reflects GKS, VDI and NAPLPS software standards
- Supports windowing, panning and scrolling
- Supports drawing of anti-aliased vectors, circles and arcs with various user-definable line styles
- Fills arbitrary polygons
- Supports dual-port video DRAMs
- CMOS technology
- Provides memory and video refresh at user-definable rates
- Interfaces to any 8 or 16-bit system bus
- Comprehensive instruction set
- 145-pin PGA package

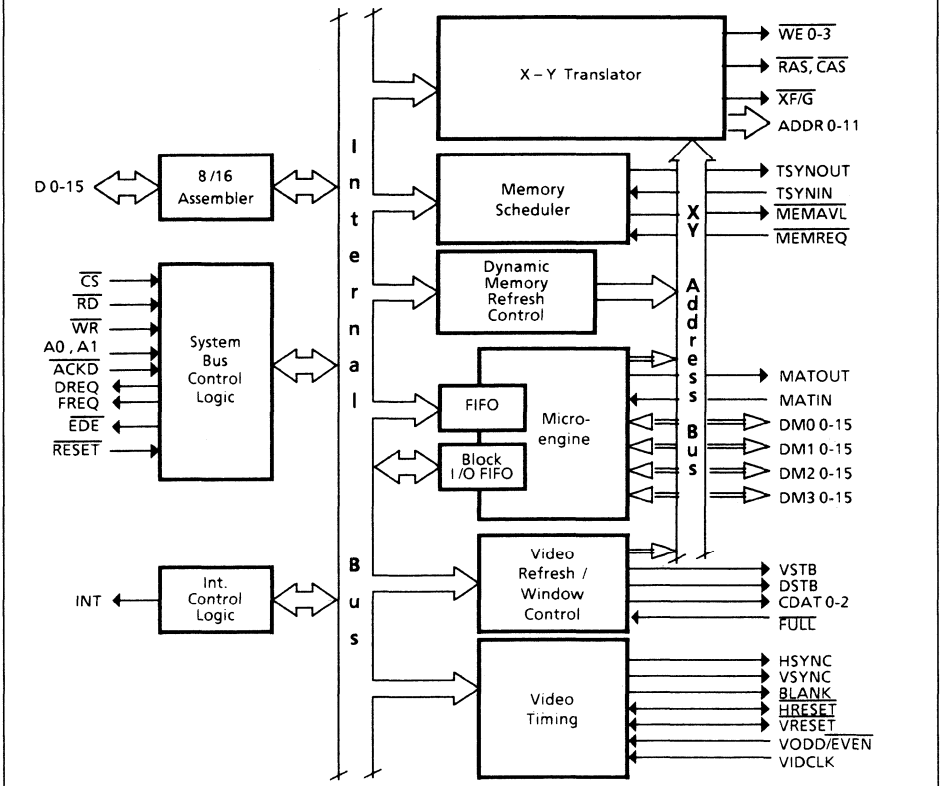
Logic Symbol



The Siemens SAB 95C60 Quad Pixel Dataflow Manager (QPDM) is a CMOS graphics processor which contains the necessary circuitry and control functions for driving four bit-mapped memory arrays. Featuring a maximum system clock speed of 20 MHz, the SAB 95C60 can interface to any 8 or 16-bit system bus, and can draw vectors at a speed of up to 3.3 million pixels per second or place text at a rate of 50,000 characters per second. Such performance allows the user to efficiently mix text and graphics within the bit map. The SAB 95C60 QPDM also contains graphics primitives which smoothly interface with the GKS, VDI and NAPLPS software standards.

9.87

Block Diagram

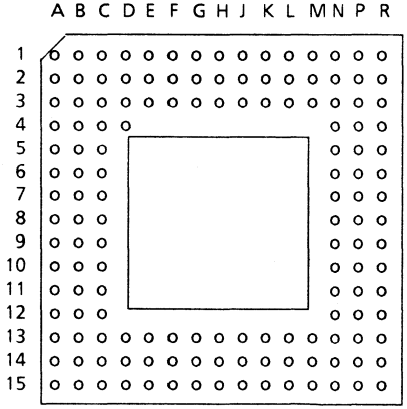


Pin Configuration

Pin Grid Array Package
Bottom view

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	DM3 14	DM3 13	DM3 11	DM3 10	DM3 7	DM3 5	DM3 3	DM3 1	TEST	DM0 12	DM0 10	DM0 9	DM0 7	DM0 5	DM0 1	1
2	DM2 0	DM3 15	DM3 12	DM3 8	DM3 4	DM3 2	DM3 0	MATOUT	DM0 14	DM0 13	DM0 11	DM0 8	DM0 2	DM0 3	DM0 0	2
3	DM2 2	DM2 4	DM2 1	DM3 9	GND	DM3 6	+ 5V	MATIN	+ 5V	DM0 15	GND	DM0 6	DM0 4	DM1 4	DM1 0	3
4	DM2 6	DM2 7	DM2 5	NC									DM1 1	DM1 3	DM1 2	4
5	DM2 9	DM2 11	DM2 3										DM1 7	DM1 6	DM1 5	5
6	DM2 13	DM2 8	GND										GND	DM1 8	DM1 9	6
7	DM2 15	DM2 12	DM2 10										DM1 14	DM1 10	DM1 11	7
8	DM2 14	ADDR10	ADDR11										DM1 12	DM1 13	DM1 15	8
9	ADDR 8	ADDR 9	GND										GND	D 14	D 15	9
10	ADDR 6	ADDR 5	+ 5V										D 13	D 12	D 11	10
11	ADDR 4	ADDR 7	ADDR 1										GND	D 10	D 9	11
12	ADDR 3	ADDR 2	GND										D 8	D 7	D 6	12
13	FULL	ADDR 0	RAS	WE 0	CAS	XF/G	+ 5V	VODD /EVEN	DREQ	INT	+ 5V	WR	D 5	D 3	D 4	13
14	VSTB	CDAT 2	CDAT 0	WE 1	TSYNIN	MEMAVL	VSYNC	BLANK	HRESET	SYSCLK	RESET	RD	ACKD	D 1	D 2	14
15	DSTB	CDAT 1	WE 3	WE 2	TSYNOUT	MEMREQ	HSYNC	VRESET	VIDCLK	FREQ	A 0	A 1	CS	EDE	D 0	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

PGA Package
Bottom view



Pin Names in Alphabetical Order

Pin Name/ Function	Pin
A0	L15
A1	M15
ADDR 00	B13
ADDR 01	C11
ADDR 02	B12
ADDR 03	A12
ADDR 04	A11
ADDR 05	B10
ADDR 06	A10
ADDR 07	B11
ADDR 08	A9
ADDR 09	B9
ADDR 10	B8
ADDR 11	C8
$\overline{\text{ACKD}}$	N14
BLANK	H14
$\overline{\text{CAS}}$	E13
CDAT0	C14
CDAT1	B15
CDAT2	B14
$\overline{\text{CS}}$	N15
D00	R15
D01	P14
D02	R14
D03	P13
D04	R13
D05	N13
D06	R12
D07	P12
D08	N12
D09	R11
D10	P11
D11	R10
D12	P10

Pin Name/ Function	Pin
D13	N10
D14	P9
D15	R9
DM0 00	R2
DM0 01	R1
DM0 02	N2
DM0 03	P2
DM0 04	N3
DM0 05	P1
DM0 06	M3
DM0 07	N1
DM0 08	M2
DM0 09	M1
DM0 10	L1
DM0 11	L2
DM0 12	K1
DM0 13	K2
DM0 14	J2
DM0 15	K3
DM1 00	R3
DM1 01	N4
DM1 02	R4
DM1 03	P4
DM1 04	P3
DM1 05	R5
DM1 06	P5
DM1 07	N5
DM1 08	P6
DM1 09	R6
DM1 10	P7
DM1 11	R7
DM1 12	N8
DM1 13	P8
DM1 14	N7
DM1 15	R8

Pin Name/ Function	Pin
DM2 00	A2
DM2 01	C3
DM2 02	A3
DM2 03	C5
DM2 04	B3
DM2 05	C4
DM2 06	A4
DM2 07	B4
DM2 08	B6
DM2 09	A5
DM2 10	C7
DM2 11	B5
DM2 12	B7
DM2 13	A6
DM2 14	A8
DM2 15	A7
DM3 00	G2
DM3 01	H1
DM3 02	F2
DM3 03	G1
DM3 04	E2
DM3 05	F1
DM3 06	F3
DM3 07	E1
DM3 08	D2
DM3 09	D3
DM3 10	D1
DM3 11	C1
DM3 12	C2
DM3 13	B1
DM3 14	A1
DM3 15	B2
DSTB	A15
DREQ	J13

Pin Names in Alphabetical Order (cont'd)

Pin Name/ Function	Pin
$\overline{EDE}$	P15
FREQ	K15
$\overline{FULL}$	A13
GND	C9
GND	C12
GND	N9
GND	L3
GND	N6
GND	E3
GND	C6
GND	N11
$\overline{HRESET}$	J14
HSYNC	G15
INT	K13
MATIN	H3
MATOUT	H2
$\overline{MEMAVAL}$	F14
$\overline{MEMREQ}$	F15
NC	D4

Pin Name/ Function	Pin
$\overline{RAS}$	C13
$\overline{RD}$	M14
$\overline{RESET}$	L14
SYSCLK	K14
TEST	J1
TSYNIN	E14
TSYNOUT	E15
VIDCLK	J15
VODD/$\overline{EVEN}$	H13
$\overline{VRESET}$	H15
VSTB	A14
VSYNC	G14
V_{CC}	G3
V_{CC}	G13
V_{CC}	J3
V_{CC}	C10
V_{CC}	L13
$\overline{WE0}$	D13
$\overline{WE1}$	D14
$\overline{WE2}$	D15
$\overline{WE3}$	C15
$\overline{WR}$	M13
$\overline{XF/G}$	F13

Pin Definitions and Functions

System Bus

Symbol	Pin	Input (I) Output O)	Function
D0-D15	N10 N12, N13 P9-P14 R9-R15	I/O	COMMAND/DATA/STATUS (tristate, bidirectional) These sixteen lines are used for transferring commands/ data/status on the system bus. The nature of the information transferred on the D0-D15 lines is established in conjunction with the port address pins A0, A1.
$\overline{RD}$	M14	I	$\overline{READ}$ (input, active low) Signal used for reading information (data/status) from the SAB 95C60 QPDM on the D0-D15 lines by a bus master.
$\overline{WR}$	M13	I	$\overline{WRITE}$ (input, active low) Signal used for strobing information (commands/data) into the SAB 95C60 on the D0-D15 lines.
$\overline{CS}$	N15	I	$\overline{CHIP\ SELECT}$ (input, active low) Signal used for selecting the SAB 95C60 from several peripherals connected to the same system bus.
A0, A1	L15, M15	I	PORT ADDRESS (input, active high) These two inputs are used for selecting the appropriate port to be read or written.
SYSCLK	K15	I	SYSTEM CLOCK (input, active high) 20 MHz maximum frequency clock. Controls the SAB 95C60 QPDM internal timing exept for video timing.
INT	K13	O	INTERRUPT (output, active high) High-level interrupt output used to signal that an exception has occured. The nature of the exception can be determined by reading the status register. Execution of a write to the interrupt acknowledge register clears the INT output.
DREQ	J13	O	DATA FIFO REQUEST (output, open drain, active high) Signal used to start and suspend a transfer of data between the system memory and the display memory.
$\overline{ACKD}$	N14	I	$\overline{ACKNOWLEDGE\ DMA}$ (input, active low) The external DMA device may drive this pin low in response to a DMA request to strobe in or read out data in fly-by DMA transfer format.
FREQ	K15	O	INSTRUCTION FIFO REQUEST (output, open drain, active high) This signal is used to start and suspend a transfer of instructions from the system memory into the QPDM instruction FIFO.

Pin Definitions and Functions (cont'd)

System Bus (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{EDE}}$	P15	O	$\overline{\text{EXTERNAL DRIVER ENABLE}}$ (output, active low) This pin is used to enable external data bus drivers on the system bus and is inactive (high) during an output block operation on those SAB 95C60 devices that do not participate in the output. This signal eliminates contention on the system bus.
MATOUT	H2	O	MATCH OUT (output, active high) This pin is used in a multiple QPDM application to search for a matching pattern. As long as the pattern is not found, this pin stays low. When the matching pattern is found, the pin is driven high. Since all the MATOUT outputs are logically ANDed externally, a match in a multiple QPDM environment is visible on MATIN when all the MATOUT outputs are high. This pin is also used for instruction execution synchronization by re-aligning the SAB 95C60 devices in a system at the beginning of each instruction execution and at the beginning of each word transfer in a block I/O instruction.
MATIN	H3	I	MATCH IN (input, active high) This pin is connected to the output of the AND gate connected to the MATOUT outputs.
TSYNOUT	E15	O	TIMING SYNCHRONIZATION (output, active high) In conjunction with TSYNIN, this pin is used to synchronize display memory bus activities. The TSYNOUT pins of all SAB 95C60 devices in a system are ANDed together and connected (optionally buffered) to the TSYNIN input pins of all SAB 95C60s. User-transparent information signals all SAB 95C60 devices about display memory bus activities.
TSYNIN	E14	I	TIMING SYNCHRONIZATION (input, active high) All TSYNIN input pins are connected to the TSYNOUT junction, or to the output of the optional buffer.
$\overline{\text{RESET}}$	L14	I	$\overline{\text{SYSTEM RESET}}$ (input, active low) The $\overline{\text{RESET}}$ signal brings all SAB 95C60s in the system to the same initial state. All the outputs are brought into the inactive state. If this pin is activated while the SAB 95C60 is active, all activities will be suspended.
TEST	J1	I	TEST INPUT Must be grounded.

Pin Definitions and Functions (cont'd)

Display Memory Bus

Symbol	Pin	Input (I) Output (O)	Function
ADDR 0–11	A9–A12 B8–B13 C8, C11	O	ADDRESS (output, active high) The twelve lines of ADDR are used for addressing bit-map planes each up to 4 K × 4 K bits. The addresses are multiplexed and contain row and column addresses and bank-select bits.
DM0 0–15 DM1 0–15 DM2 0–15 DM3 0–15		I/O	DISPLAY MEMORY BUS (bidirectional) These 64 lines are used for transferring data between the SAB 95C60 and the display memory. There are sixteen lines for each of the four planes.
$\overline{RAS}$	C13	O	$\overline{ROW\ ADDRESS\ STROBE}$ (output, active low) This line is used for strobing the memory planes to be read or written to at the address on ADDR (row address).
$\overline{CAS}$	E13	O	$\overline{COLUMN\ ADDRESS\ STROBE}$ (output, active low) This line is used for strobing the memory planes to be read or written to at the address on ADDR (column address).
$\overline{XF/G}$	F13	O	$\overline{TRANSFER/OUTPUT\ ENABLE}$ (output, active low) This pin interfaces directly to the video DRAM. During a transfer cycle this pin indicates a transfer to the video DRAMs. During a random read cycle, this pin enables the output buffer of the video DRAMs.
$\overline{WE\ 0}$ – $\overline{WE\ 3}$	D13–D15 C15	O	$\overline{WRITE\ ENABLE}$ (output, active low) The $\overline{WE}$, when active, signifies that the current transaction on the display memory bus is a write to the corresponding bit plane.
$\overline{MEMREQ}$	F15	I	$\overline{MEMORY\ REQUEST}$ (input, active low) This asynchronous signal is used by an external device to request access to the display memory bus.
$\overline{MEMAVL}$	F14	O	$\overline{MEMORY\ BUS\ AVAILABLE}$ (output, active low) This line is used to inform external devices requesting the bus that the SAB 95C60 is not driving the data lines.

Pin Definitions and Functions (cont'd)

Video Control Bus

Symbol	Pin	Input (I) Output (O)	Function
VODD/$\overline{\text{EVEN}}$	H13	I	VERTICAL ODD/$\overline{\text{EVEN}}$ (input) This input is optionally used in the interlaced display mode to distinguish between the even frame and the odd frame produced by an external device synchronized with the SAB 95C60.
VSTB	A14	O	VIDEO STROBE (output, active high) This strobe signal is used in a system with video dynamic RAMs (VRAMs) and an external VDAF (AM8171/8172 discrete components) to shift video data out of the video memory. With every strobe, a 16-bit word is shifted out of the video memory.
DSTB	A15	O	DATA STROBE (output, active high) This strobe signal loads 8 bits of video data into the VDAF. DSTB is synchronous to SYSCLK and has twice the frequency of VSTB.
CDAT 0–2	B14, B15 C14	O	CONTROL DATA (output, active high) These lines are used to output three bits of information to the VDAF. Information is sent to the VDAF during the transfer cycle.
$\overline{\text{FULL}}$	A13	I	$\overline{\text{FULL}}$ (input, active low) This input alerts the SAB 95C60 that the VDAF cannot accept more video data. If the $\overline{\text{FULL}}$ signal is active, the SAB 95C60 stops generating the VSTB and DSTB signals.
VIDCLK	J15	I	VIDEO CLOCK (input) 15 MHz maximum frequency clock. This clock signal is used for generating video synchronization signals and for loading the video serialization registers.
HSYNC	G15	O	HORIZONTAL SYNC (output, active high) HSYNC is an active high output used to cause horizontal retrace of the CRT's electron beam. This output is held low when the SAB 95C60 is reset to prevent any uncontrolled synchronization to the CRT which may cause damage of the tube.
VSYNC	G14	O	VERTICAL SYNC (output, active high) VSYNC is an active high output used to cause vertical retrace of the CRT's electron beam. This output is held low when the SAB 95C60 is reset.
BLANK	H14	O	BLANK VIDEO (output, active high) BLANK is an active high output which serves to blank out inactive display areas of the CRT. This output is held high when the SAB 95C60 is reset.

Pin Definitions and Functions (cont'd)

Video Control Bus (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{HRESET}}$	J14	I/O	$\overline{\text{HORIZONTAL RESET}}$ (bidirectional, active low) This pin is an output for horizontal video masters, and an input for horizontal video slaves. It is used for horizontal video synchronization to other SAB 95C60 devices or to an external video source.
$\overline{\text{VRESET}}$	H15	I/O	$\overline{\text{VERTICAL RESET}}$ (bidirectional, active low) This pin is an output for vertical video masters and an input for vertical video slaves. It is used for vertical video synchronization to other SAB 95C60 devices or to one external video source.

Power Connections

Symbol	Pin	Function
V_{CC}	C10, G3 G13, I3 L13	POWER SUPPLY Each V_{CC} must be connected to + 5 V power supply.
GND	C6, C9 C12, E3 L3, N6 N9, N11	GROUND Each GND pin must be connected to the power supply ground.

Functional Description

The SAB 95C60 quad pixel dataflow manager is a graphics processor which maintains, updates and displays information on four bit-mapped video planes. As depicted in the figure below, the system interface communicates with either an 8 or 16-bit host CPU while the display memory interface controls four bit-mapped memory planes. These planes consist of dual-port video dynamic memories (VRAMs). The SAB 95C60 connects VRAMs to the random ports while the serial ports are used as access to video information for the screen refresh. When used in conjunction with a video data assembly FIFO, the SAB 95C60 is capable of displaying a hardware window with the associated features of smooth pan and soft scroll.

The SAB 95C60 QPDM performs three fundamental functions described as follows:

Video Refresh

The SAB 95C60 QPDM manages the screen (display) refresh function by generating the addresses to the bit-mapped VRAMs as required to access data for display on the screen. The data from the VRAMs is serialized externally to the SAB 95C60.

The video refresh operation is fully programmable allowing the user to tailor the system as required. The screen display can be aligned on any pixel boundary and can also include one hardware window overlay. Additionally, the total video process can be externally synchronized to any external source at the horizontal or vertical synchronization rate. Video refresh can be disabled for operation as a slave device.

Dynamic Memory Refresh

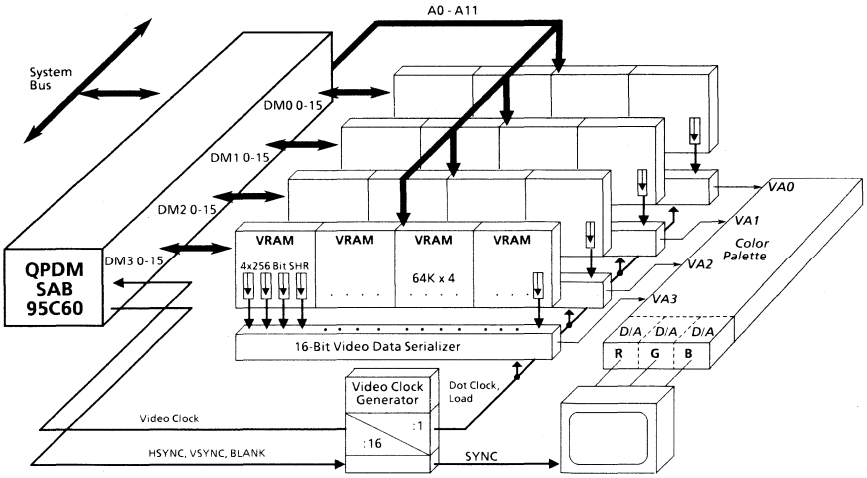
The SAB 95C60 performs the dynamic memory refresh function for the display memory. The dynamic memory refresh process is interleaved with the video refresh and with the display memory updating. The refresh rate can be programmed by loading the 10-bit dynamic memory refresh rate register.

This register holds the number of SYSCLK cycles between two refresh cycles.

The dynamic memory refresh rate register is loaded into a counter, which is counted down by the SYSCLK. When the counter reaches its zero state, it sends a refresh request to the memory scheduler. As soon as the memory scheduler arbitrates a time slice for the dynamic memory refresh block, a refresh cycle is initiated.

The SAB 95C60 executes $\overline{CAS}$ before $\overline{RAS}$ refresh cycles.

Typical QPDM Graphics System



Display Memory Update

The SAB 95C60 has access to the display memory bus for updating purposes, except for those times when it is performing video or dynamic memory refresh.

Placing an instruction in the execution FIFO (see block diagram) signals the microengine to begin operation. If the execution of the instruction requires access to the display memory bus (this is the case in most instructions), the SAB 95C60 continues the instruction execution unless the display memory bus is occupied by the video refresh or the dynamic memory refresh process. If the display memory bus cannot be accessed momentarily, the execution is suspended until the display memory is available.

The drawing instruction set includes line, circle, fill polygon, string and many others which will be briefly described in the following.

Feature Description

Window Display Mechanism

The SAB 95C60 QPDM, in conjunction with a video data assembly FIFO (VDAF) or an equivalent device, can support a single non-destructive hardware window. The image to appear in the window is located in some other area of the display memory than that visible on the screen. The size and position of the window is programmed into a set of registers on the SAB 95C60. Since the window position is dynamically programmable, it is easy to 'drag' a rectangular area containing an object. It is also easy to perform soft scrolling and smooth panning of either background or foreground.

The window may be positioned arbitrarily on the screen and it may be of any size. Final serialization cannot occur until data from the background has window. Five signals are provided to control a data assembler.

$\overline{\text{MEMREQ}}$ and $\overline{\text{MEMAVL}}$ are used to allow another processor direct access to the display memory.

Clipping

The clipping feature on the SAB 95C60 allows a rectangular region to be defined outside of which vectors and arcs will not be drawn, blocks will not be moved or modified, and polygons will not be filled. The clipping window is specified by the user, and remains in effect until changed or disabled.

Picking

If a drawing consists of a large number of objects and each object is defined by a number of drawing primitives, any object can be identified by the following picking process:

First, the picking area is defined as a rectangular region in display memory. Whenever a drawing intersects the picking area, a "pick detect" bit in the status register is set. Objects to be displayed are labeled by using the signal instruction which will return the label of the object that intersected the picking area.

String Mode

The SAB 95C60 QPDM has the capability of generating alphanumerics and so-called "character graphics" efficiently and with a minimum of user intervention. This capability is referred to as "string mode".

In string mode, the user issues a string of 16-bit characters which are then written into the bit map. Before using this mode, the user must load a "font" into the display memory. All mixing of text and graphics is accomplished within the display memory. Character patterns generated in this manner can be of arbitrary size and alignment.

Multiple SAB 95C60 Operation

In order to accommodate systems requiring access to more than four bit planes, the SAB 95C60 is designed to be fully cascadable with no performance degradation. Multiple SAB 95C60 devices can communicate with each other to share timing information for synchronization purposes, and status information for color comparisons in depth.

Instructions that are to be executed are transmitted to all SAB 95C60 devices at once. Each plane will use the instruction in conjunction with its own activity and color bits to decide whether to execute or to ignore the instruction. Each plane may execute the instruction differently, depending on the contents of the individual memory plane and the contents of plane-specific status information.

Transmission is accomplished by selecting all SAB 95C60 QPDMs simultaneously and writing to port 0. (Write to the instruction FIFO.)

TSYNOUT and TSYNIN are used to synchronize display memory operations in a multiple SAB 95C60 system.

MATOUT and MATIN are used to exchange color searching information in a multiple SAB 95C60 device system and to synchronize instruction execution.

Interface Description

System Bus Interface

The host is connected to the system side of the SAB 95C60 as depicted in the logic symbol diagram. There is a 16-bit data path, and the 8 or 16-bit option allows the SAB 95C60 to be connected to an 8 or 16-bit host processor.

The normal bus interface control lines are supported through $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ and two address bits. The address bits are decoded to select one of four ports:

A1	A0	Write Function	Read Function
0	0	Write Instruction FIFO	Read Status
0	1	Write Block Input FIFO	Read Block Output FIFO
1	0	Write Register Address	Read Register Address
1	1	Write Register	Read Register

The SAB 95C60 QPDM can be supported with a DMA controller allowing blocks of information or instructions to be transferred without tying up the host. In addition to the normal flow-through DMA operations, the SAB 95C60 also supports fly-by operations.

The SAB 95C60 can also use interrupts to signal the occurrence of certain events. Some events are repetitive (e.g. frame), some indicate error conditions (e.g. stack overflow), and some merely report status (e.g. idle). There are registers for masking interrupts, reading interrupt requests and acknowledging interrupts.

Display Memory Bus Interface

On the display memory side, the SAB 95C60 is capable of controlling four bit planes. Addresses, $\overline{RAS}$ and $\overline{CAS}$ are common signals to all bit planes while each plane has its own set of data lines and write enable ($\overline{WE}$). Typically, eight or nine address lines (multiplexed row/column) go to the VRAM devices while the others may be used for bank select. If multiple banks of memory are used, row addresses are decoded to select the proper bank.

Each bit plane has a 16-bit data bus used for the display memory update function. Typically, to write a single pixel (one bit in each plane), the SAB 95C60 would perform simultaneous 16-bit reads from all planes, followed by simultaneous 16-bit writes to all planes. Logic is also provided in the SAB 95C60 to perform individual pixel writes.

The SAB 95C60 is intended to be used with a variety of dual-ported video RAMs. Prior to the beginning of each scan line, the SAB 95C60 executes a transfer cycle which copies the contents of the scan line into shift registers on the VRAM devices. The scan line image is then shifted out of the VRAM devices 16 bits at a time and further serialized at the dot clock rate for display purposes. The primary VRAM port is available during this time for display memory update.

Display Memory/RAM Size Examples

Bit Map Size	VRAM Size	VRAMs/ Plane	VRAMs/ SAB 95C60
1024 × 1024	64K × 4	4	16
1024 × 2048	64K × 4	8	32
2048 × 2048	64K × 4	16	64
4096 × 4096	256K × 4	16	64

Video Bus Interface

The SAB 95C60 generates video timing. Horizontal timing is programmed in terms of VIDCLK cycles and vertical timing is programmed in terms of scan lines.

$\overline{HRESET}$ and $\overline{VRESET}$ are either inputs or outputs depending on the SAB 95C60 master/slave status. In the case where multiple SAB 95C60s control the display, one SAB 95C60 would be programmed as the timing master and the others would be programmed as timing slaves.

Performance Figures

Working with VRAMs, the SAB 95C60 can easily manage high-resolution screen formats requiring dot clock rates up to 240 MHz.

Moreover, it performs the bit-map update function as indicated in the table below:
The SAB 95C60 provides extremely fast access at the host interface. A host write requires as little as 80 ns, while a register may be read in as little as 120 ns.

Performance Figures of SAB 95C60

Instruction	Instruction Overhead	Intermediate Overhead	Execution Time	Comments
Line	12.9 µs	(not applicable)	300 ns/Pixel	
Line	12.9 µs	(not applicable)	4750 ns/Pixel	Anti-Aliased
Polyline	10.6 µs	4.8 µs/Segment	300 ns/Pixel	Connected Segments
Arc	28.2 µs	2.7 µs/Octant	750 ns/Pixel	
Arc	28.2 µs	2.7 µs/Octant	4750 ns/Pixel	Anti-Aliased
Circle	9.9 µs	2.7 µs/Octant	750 ns/Pixel	
Circle	9.9 µs	2.7 µs/Octant	4750 ns/Pixel	Anti-Aliased
Copy Block	10.9 µs	1.8 µs/Scan Line	55 ns/Pixel	BITBLT
Transform Block	11.0 µs	(included)	1280 ns/Pixel	3x Zoom
Seed Fill	10.0 µs	12.1 µs/Scan Line	280 ns/Pixel	Intermediate Overhead Varies with Shape
Filled Rectangle	11.9 µs	2.2 µs/Scan Line	19 ns/Pixel	Graphical Set
Filled Triangle	54.9 µs	8.0 µs/Scan Line	19 ns/Pixel	Intermediate Overhead Varies with Shape
String	6.3 µs	9.4 µs/Character	2000 ns/Scan Line	

Register Description

The SAB 95C60 QPDM contains a number of registers which are programmable by the host. These registers are listed below:

Video Control uses eight registers which define video operation parameters:

- Horizontal Sync Pulse Width (HSYNC)
- Horizontal Scan Delay (HDEL)
- Horizontal Active Pixels (HACT)
- Horizontal Total Count (HTOT)
- Vertical Sync Pulse Width (VSYNC)
- Vertical Scan Delay Odd (VDELODD)
- Vertical Scan Delay Even (VDELEVEN)
- Vertical Active Lines (VACT)
- Vertical Total Lines (VTOT)

Visible Screen Coordinates use four registers which contain the (x,y) address in real memory of the top-left and bottom-right corner of the visible screen in display memory:

- Screen X Start
- Screen Y Start
- Screen X Terminate
- Screen Y Terminate

Window Control uses six registers which specify where the window is located on the screen (the apparent window) and where it begins in memory (the real window):

- Window Apparent X Start
- Window Apparent Y Start
- Window Apparent X Terminate
- Window Apparent Y Terminate
- Window Real X
- Window Real Y

Video Mode Register is used to indicate to each SAB 95C60 whether it is a timing master or slave, and whether or not interlaced display mode is to be used.

Memory Mode Register specifies display memory configuration in terms of memory width and device size (e.g. 4K wide/256 K devices).

Dynamic Memory Refresh Rate Register specifies the number of SYSCLK clock cycles between row refreshes in dynamic memory refresh.

Interrupt Mask Register indicates which conditions are allowed to cause interrupts to the host.

Video Timing Enable is a 1-bit register used to enable and disable video sync and output.

Video Refresh Enable is a 1-bit register used to enable and disable the collection of the video information from the display RAM.

Interrupt Acknowledge Register indicates that a specific interrupt condition is known to the host and that the request is to be cancelled in the SAB 95C60.

System Bus Width Register configures the SAB 95C60 to 8-bit or 16-bit-system bus modes.

Instruction Set

The SAB 95C60 QPDM is a graphics processor with a powerful instruction set. Most of the graphics instructions can be specified with respect to several addressing modes, relative to screen position, pen position, and absolute memory. The SAB 95C60 QPDM instructions are briefly described in the following:

Arc draws the image of a circular arc in display memory. The input parameters are the center of the arc, the radius of the arc and the two end-points. The image may be drawn using anti-aliasing.

Arc Current draws the image of a circular arc in display memory. It is similar to "arc" except the center is taken to be the current pen position (rather than being specified).

Call begins fetching instructions from display memory rather than from the instruction FIFO. The parameters specify the location of the program to be called. A stack in display memory is used to contain the return location. The call instruction may also be indexed or conditional.

Circle draws the image of a circle in display memory. The input parameters are the circle's center and radius. The image can be drawn using anti-aliasing.

Circle Current draws the image of a circle in display memory. It is similar to "circle", except that the center is taken to be the current pen position.

Control Clipping enables or disables the clipping function. When clipping is enabled, all drawing primitives will change only that portion of display memory which lies within the rectangular clipping region.

Control Picking enables or disables the picking function. When picking is enabled, drawing primitives will not execute any writes to the display memory. The pick detect status bit is set whenever a drawing primitive intersects the picking area.

Copy Block moves a block of data within display memory and may optionally perform logical operations on the data. The size of the block will have been determined by a "set block size" instruction. The location of each block, source and destination, is determined by the instruction.

Copy Block Current is identical to the "copy block" instruction except that the source operand is the current pen position.

Define Logical Pel specifies the logical pel (pen size) used by the drawing primitives. This can be used to draw thick lines.

Fill Bounded Region fills an arbitrary polygon with a specific color. The polygon is defined as the group of dots connected to the seed point and completely contained within a boundary of pixels of the edge color. All pixels connected to the seed point will be changed to the current drawing color. The location of the seed is specified in the instruction.

Fill Bounded Region Current fills an arbitrary polygon with a specific color. The polygon is defined as the group of dots connected to the seed point and completely contained within a boundary of pixels of the edge color. All pixels connected to the seed point will be changed to the current drawing color. The location of the seed is the current pen position.

Fill Connected Region fills an arbitrary polygon with a specific color. The polygon is defined as any group of connected dots of the seed's color. All pixels connected to the seed point having the same color will be changed to the current drawing color. The location of the seed is specified in the instruction.

Fill Connected Region Current fills an arbitrary polygon with a specific color. The polygon is defined as any group of connected dots of the seed's color. All pixels connected to the seed point having the same color will be changed to the current drawing color. The location of the seed is the current pen position.

Filled Rectangle creates the image of a rectangle and fills it. The parameters specify two opposite corners of the rectangle. The color of the filled rectangle is the current drawing color.

Filled Rectangle Current is similar to "fill rectangle" except the current pen position is taken to be the starting corner of the rectangle. The other corner is specified by the instruction.

Filled Triangle creates the image of a triangle and fills it. The parameters specify the three vertices of the triangle. The color of the filled triangle is the current drawing color.

Filled Triangle Current creates the image of a triangle and fills it. The parameters specify two vertices of the triangle. The current pen position is taken to be the initial vertex of the triangle. The color of the filled triangle is the current drawing color.

Input Block transfers a rectangular block of data from the host to display memory. The size of the block will have been determined by a "set block size" instruction. The destination address in the display memory is specified in the instruction. The data to be stored in display memory is written into the data FIFO.

Input Block Current transfers a rectangular block of data from the host to display memory. The size of the block will have been determined by a "set block size" instruction. The destination address in the display memory is the current pen position. The data to be stored in display memory is written into the data FIFO.

Jump unconditionally changes the location counter when executing instructions from display memory. The jump instruction may also be indexed or conditional.

Line (Polyline) draws the image of a line in display memory. The input parameters are the two ends of the line. The image may be drawn using anti-aliasing.
Polylines may be drawn, setting a special bit within the end point parameters. In this way, the QPDM is forced to fetch more parameters to continue line drawing.

Line Current is similar to "line", except the current drawing position is taken to be the starting point of the line.

Move Pen sets the current pen position.

No Operation ensures that no operation is performed.

Output Block transfers a rectangular block of data from display memory to the host. The size of the block will have been determined by a "set block size" instruction. The source address in the display memory is specified in the instruction. The host is expected to remove the data from the data FIFO.

Output Block Current transfers a rectangular block of data from display memory to the host. The size of the block will have been determined by a "set block size" instruction. The source address in the display memory is the current pen position. The host is expected to remove the data from the data FIFO.

Point (Polypoint) draws the image of the current logical pel at the location specified in the instruction. Polypoints may be drawn, setting a special bit within the point parameters. In this way, the QPDM is forced to fetch more parameters to continue point drawing.

Point Current draws the image of the current logical pel at the current pen position.

Pop Current Pen Position causes the internal current pen position to be popped from the display memory stack.

Push Current Pen Position causes the internal current pen position to be pushed on the display memory stack.

Return exits from a subroutine or from program mode when executing instructions from display memory.

Set Activity Bits indicates which of the four display memory planes, controlled by the SAB 95C60, are to be written into.

Set Anti-Aliasing Distance programs the anti-aliasing distance deviation from the ideal line.

Set Block Size specifies the number of pixels moved in a block move operation. This is used for input block, output block, copy block, and transform block.

Set Character Font Base specifies the character font address in the display memory. The character font contains the patterns of letters and numbers used in the "string" instruction.

Set Clipping Boundary specifies where the clipping region is in display memory. When clipping is enabled, all drawing primitives will change only that portion of display memory which lies within the rectangular clipping region. The parameters are the addresses of two opposite corners of the clipping rectangle.

Set Clipping Boundary Current specifies where the clipping region is in display memory. When clipping is enabled, all drawing primitives will change only that portion of display memory which lies within the rectangular clipping region. The current pen position is taken to be the start corner of the clipping rectangle.

Set Color Bits defines the current drawing color.

Set Search Color specifies the edge color used in "fill" instructions.

Set Line Style specifies the line style. This defines the dash length, the interspace length, and the dot length.

Set Line Style Phase indicates where the line style begins within the line.

Set Listen Bits indicates which planes take part in polygon and color change operations. If reset, the corresponding plane doesn't participate in the color matching.

Set Picking Region specifies the rectangular area to be picked. The parameters are two opposite corners of the picking rectangle. When picking is enabled, drawing primitives that intersect the picking region will cause the "pick detect" bit in the status register to be set and no writes will be executed to display memory.

Set Picking Region Current specifies the rectangular area to be picked. The parameters are two opposite corners of the picking rectangle. The current pen position is taken to be the start corner of the picking region. When picking is enabled, drawing primitives that intersect the picking region will cause the "pick detect" bit in the status register to be set and no writes will be executed to display memory.

Set QPDM Position specifies the logical addresses for the display memory planes in systems with multiple QPDMs.

Set Scale Factor loads the scale factor register with values used to multiply the operands of instructions which address the bit map.

Set Stack Boundaries specifies to the SAB 95C60 which area of display memory has been set aside for the stack. Stack overflow is detected and signaled to the host with an interrupt.

Signal is used to indicate to the host when a particular point in the instruction stream has been reached, to delimit objects during picking, or to pause operation waiting for a signal from the host.

Store Immediate deposits a specified number of 16-bit words in the display memory. The pointer may be used by one of the indirect addressing modes.

Store Current Pen Position stores the internal current pen position at the location specified in the instruction.

String is used to create the image of a string of text in the display memory. The parameters are the address at which the string should begin, followed by a variable length list of 16-bit pointers. Each pointer is used to look up a pattern in the character font table.

String Current is similar to "string" except the address at which the string should begin is set to the current pen position.

Transform Block allows a block of data to be taken from display memory, operated on and written to a different area of display memory. The operations which may be performed are rotate (90 degree increments), zoom (by pixel replication), and mirror. The zoom in X-direction and zoom in Y-direction are independently specified. The size of the source block (prior to rotation and zooming) will have been specified as "set block size" instruction.

Transform Block Current is similar to "transform block" except the source operand is at the current pen position.

Absolute Maximum Ratings

Storage temperature	−65°C to + 125°C
Ambient operating temperature	−55°C to + 125°C
Maximum V_{CC} relative to V_{SS}	−0.3V to + 7.0V
DC voltage applied to any input with respect to V_{SS}	−1.0V to V_{CC} + 0.3V
DC voltage applied to any output pin with respect to V_{SS}	−0.5V to V_{CC} + 0.3V

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

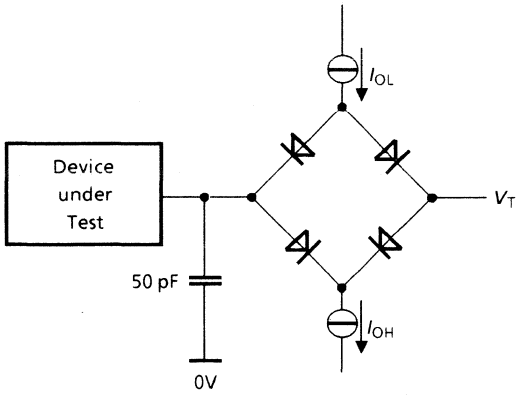
DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 5%

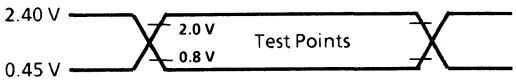
Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.3	+0.8	V	–
V_{IH}	Input high voltage	+2.0	V_{CC}+0.3	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.0 mA
	($\overline{CAS}$ and $\overline{XF/G}$)	–	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage	2.4	–	V	I_{OH} = 250 µA
I_{OL}	Output leakage current	–	±10	µA	0.4<V_{OUT}<V_{CC}
I_I	Input current	–	±10	µA	0.4<V_{IN}<V_{CC}
C_{IN}	Input capacitance	–	20	pF	–
C_{IO}	I/O capacitance	–	20	pF	–
C_{OUT}	Output capacitance	–	15	pF	

AC Testing

Standard Test Load



I/O Waveforms



AC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5%

System Bus Timing

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_1	Requires that the addresses be valid a minimum of {} ns before $\overline{CS}$ begins to fall.	0	–	0	–	0	–	ns
t_2	Requires that both $\overline{CS}$ and $\overline{ACKD}$ be not active a minimum of {} ns before either can go active. 1)	65	–	95	–	125	–	ns
t_3	Guarantees that DREQ will not become active a maximum of {} ns after $\overline{RD}$ or $\overline{WR}$ becomes active.	–	50	–	60	–	70	ns
t_4	Guarantees that $\overline{EDE}$ will become active a maximum of {} ns after $\overline{CS}$ becomes active. Also guarantees that $\overline{EDE}$ will become active a maximum of {} ns after $\overline{ACKD}$ becomes active. 1)	–	50	–	60	–	70	ns
t_5	Guarantees that $\overline{EDE}$ will remain active a minimum of {} ns after $\overline{CS}$ has become inactive. Also guarantees that $\overline{EDE}$ will remain active a minimum of {} ns after $\overline{ACKD}$ has become inactive. 1) 3)	10	–	10	–	10	–	ns
t_6	Guarantees that $\overline{EDE}$ will have gone inactive no more than {} ns after $\overline{CS}$ has become inactive. Also guarantees that $\overline{EDE}$ will have gone inactive no more than {} ns after $\overline{ACKD}$ has become inactive.	–	65	–	70	–	75	ns
t_7	Requires that $\overline{CS}$ be valid a minimum of {} ns before $\overline{RD}$ can begin to go active. Also requires that $\overline{ACKD}$ be valid a minimum of {} ns before $\overline{WR}$ can begin to go active. 1) 2)	0	–	0	–	0	–	ns
t_8	Requires that the address remains valid a minimum of {} ns after $\overline{RD}$ has gone inactive.	10	–	10	–	10	–	ns
t_9	Requires that $\overline{CS}$ remains active a minimum of {} ns after $\overline{RD}$ has gone inactive.	0	–	0	–	0	–	ns

For notes refer to page 374.

System Bus Timing (cont'd)

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{10}	Guarantees that the read data will be valid within {} ns of $\overline{RD}$ becoming active. Also guarantees that the read data will be valid within {} ns of $\overline{WR}$ becoming active in a fly-by read cycle. 2)	–	110	–	110	–	120	ns
t_{11}	Guarantees that the read data will remain valid a minimum of {} ns after $\overline{RD}$ has gone inactive. Also guarantees that the read data will remain valid a minimum of {} ns after $\overline{WR}$ has gone inactive in a fly-by read cycle. 2) 3)	10	–	10	–	10	–	ns
t_{12}	Guarantees that the read buffers will begin to enter high impedance within {} ns of $\overline{RD}$ having gone inactive. Also guarantees that the read buffers will begin to enter high impedance within {} ns of $\overline{WR}$ having gone inactive in a fly-by read cycle. 2) 3)	–	35	–	40	–	45	ns
t_{14}	Requires that the address remains valid a minimum of {} ns after $\overline{WR}$ has gone inactive.	10	–	20	–	20	–	ns
t_{15}	Requires that $\overline{CS}$ remains active a minimum of {} ns after $\overline{WR}$ has gone inactive.	10	–	20	–	20	–	ns
t_{16}	Requires that $\overline{CS}$ is active for a minimum of {} ns before $\overline{WR}$ can begin to go active. Also requires that $\overline{ACKD}$ is active for a minimum of {} ns before $\overline{RD}$ can begin to go active in a fly-by write cycle. 1) 2)	0	–	0	–	0	–	ns
t_{17}	Requires that $\overline{WR}$ is active for a minimum of {} ns. Also requires that $\overline{RD}$ is active for a minimum of {} ns in the case of a fly-by write cycle. Also requires that $\overline{ACKD}$ remains active for a minimum of {} ns after $\overline{RD}$ has gone active in a fly-by write cycle.	70	–	90	–	110	–	ns

For notes refer to page 374.

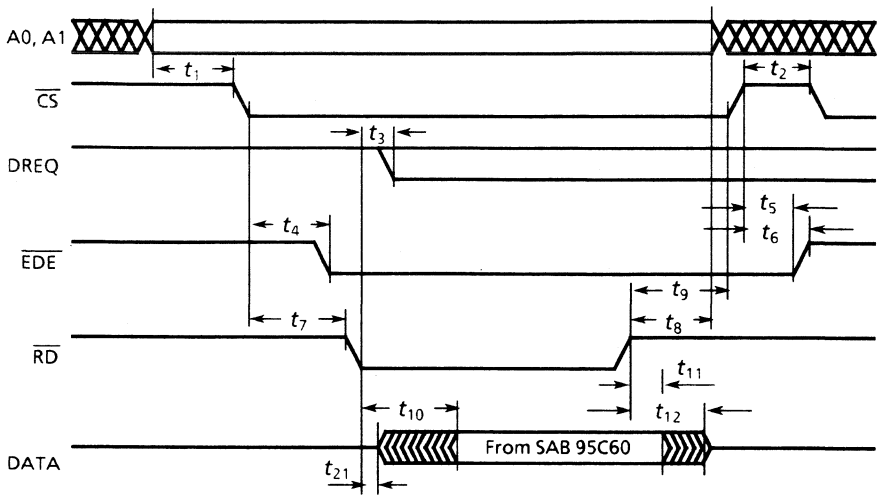
System Bus Timing (cont'd)

Symbol	Parameter		Limit values						Unit
			20 MHz		16 MHz		12 MHz		
			min.	max.	min.	max.	min.	max.	
t_{18}	Requires that the write data is active for a minimum of {} ns before $\overline{WR}$ begins to go inactive. Also requires that the write data is active for a minimum of {} ns before $\overline{RD}$ or $\overline{ACKD}$ (whichever is first) begins to go inactive in a fly-by write cycle.		50	–	75	–	100	–	ns
t_{19}	Requires that the write data is kept valid for a minimum of {} ns after $\overline{WR}$ has gone inactive. Also requires that the write data is kept valid for a minimum of {} ns after $\overline{RD}$ or $\overline{ACKD}$ (whichever is first) has gone inactive in a fly-by write cycle.	Word mode	0	–	0	–	0	–	ns
		Byte mode	15	–	25	–	25	–	ns
t_{20}	Guarantees that the INT line will become inactive no more than {} ns after $\overline{WR}$ has gone inactive.		–	120	–	150	–	180	ns
t_{21}	Guarantees that the data buffers will not become active before $\overline{RD}$ goes active. Also guarantees that the data buffers will not become active before $\overline{WR}$ goes active in a fly-by read cycle.		0	–	0	–	0	–	ns
t_{22}	Requires that $\overline{ACKD}$ is active for a minimum of {} ns after $\overline{RD}$ or $\overline{WR}$ has gone inactive		0	–	0	–	0	–	ns

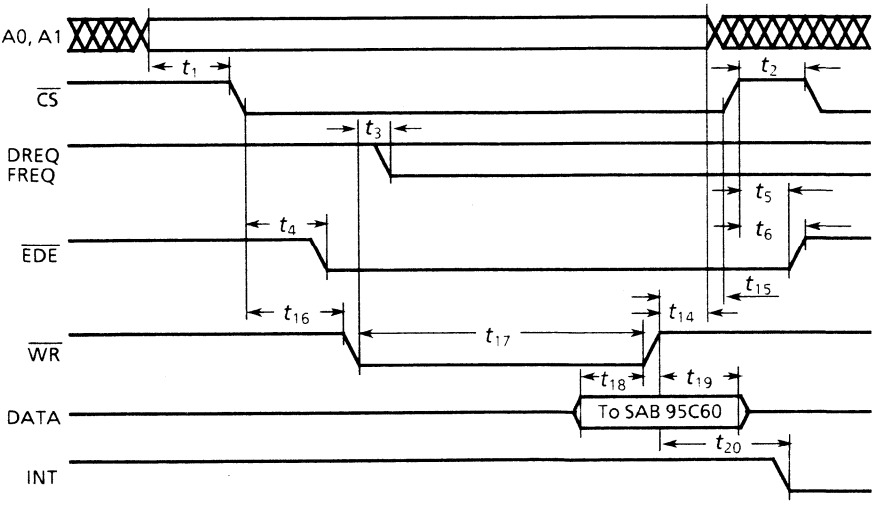
For notes refer to page 374.

System Bus Timing Waveforms

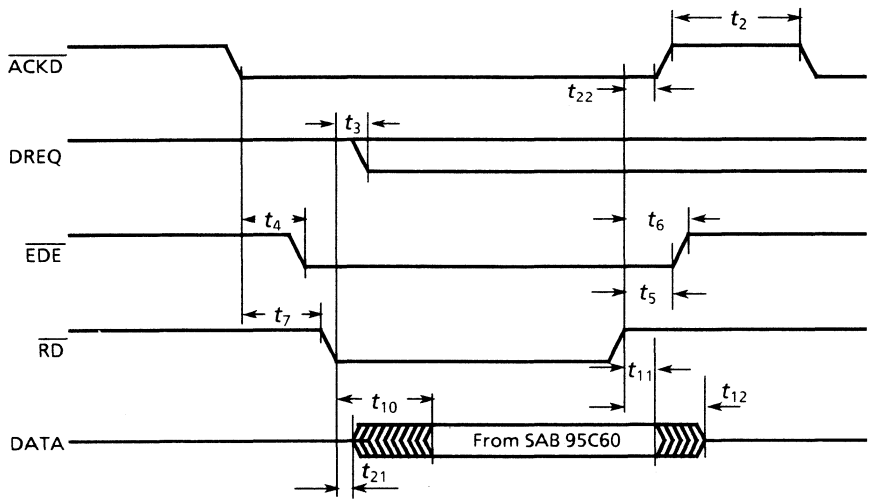
Processor/DMA Flow-Through Read Cycle



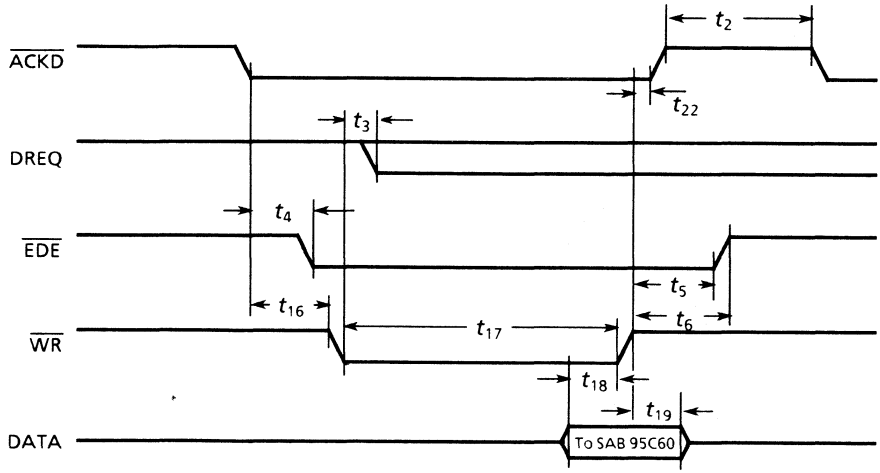
Processor/DMA Flow-Through Write Cycle



DMA Fly-by Read Cycle



DMA Fly-by Write Cycle



AC Characteristics (Notes see page 374)

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5%

Display Memory Interface Timing

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{30}	Guarantees the row address will be stable (valid) for a minimum of {} ns before $\overline{RAS}$ begins to go active. 4)	15	–	16	–	21.5	–	ns
t_{31}	Guarantees the row address will remain valid for a minimum of {} ns after $\overline{RAS}$ has gone active. 4)	35	–	45	–	63	–	ns
t_{32}	Guarantees that $\overline{XF/G}$ will not go active until a minimum of {} ns after $\overline{RAS}$ has gone active. 4)	160	–	202	–	270.5	–	ns
t_{33}	Guarantees that $\overline{RAS}$ will be active for a minimum of {} ns. 4)	180	–	225	–	307	–	ns
t_{34}	Guarantees that $\overline{RAS}$ will remain active for a minimum of {} ns after $\overline{XF/G}$ has gone inactive. 4)	14	–	15	–	21.5	–	ns
t_{35}	Guarantees that $\overline{RAS}$ will remain inactive for a minimum of {} ns. 4)	95	–	109	–	146	–	ns
t_{36}	Guarantees that $\overline{CAS}$ will not become active until a minimum of {} ns after $\overline{RAS}$ has gone active. See parameter t_{56} for write cycles. 4)	65	–	78	–	104.5	–	ns
t_{37}	Guarantees that the column address will be valid and stable for a minimum of {} ns before $\overline{CAS}$ will go active. 4)	13	–	15	–	21.5	–	ns
t_{38}	Guarantees that the column address will remain valid and stable for a minimum of {} ns after $\overline{CAS}$ has gone active. 4)	80	–	104	–	144	–	ns
t_{39}	Guarantees that $\overline{CAS}$ will be active for a minimum of {} ns in case of a read cycle or a transfer cycle. See parameter t_{57} for write cycles. 4)	100	–	130	–	180	–	ns
t_{40}	Guarantees that $\overline{CAS}$ will remain inactive for a minimum of {} ns. This is important when a refresh cycle follows any cycle. 4)	40	–	47	–	63	–	ns

Display Memory Interface Timing (cont'd)

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{41}	Guarantees that $\overline{XF/G}$ will not have gone inactive until a minimum of {} ns after $\overline{CAS}$ has gone active 4)	80	–	100	–	140	–	ns
t_{42}	Guarantees that $\overline{XF/G}$ will not be active until a minimum of {} ns after $\overline{RAS}$ has gone active. 4)	39	–	46	–	60	–	ns
t_{43}	Guarantees that $\overline{CAS}$ will remain active until a minimum of {} ns after $\overline{XF/G}$ has gone inactive. 4)	13	–	16	–	21.5	–	ns
t_{44}	Guarantees that $\overline{XF/G}$ will be active for a minimum of {} ns for a read cycle. 4)	110	–	125	–	180	–	ns
t_{45}	Requires that the read data is valid for a minimum of {} ns before $\overline{XF/G}$ begins to go inactive.	20	–	30	–	45	–	ns
t_{46}	Requires that the read data remains valid for a minimum of {} ns after $\overline{XF/G}$ has gone inactive.	0	–	0	–	0	–	ns
t_{47}	Guarantees that $\overline{RAS}$ will not begin to go active until a minimum of {} ns after $\overline{CAS}$ has become active in a refresh cycle. 4)	37	–	45	–	63	–	ns
t_{48}	Guarantees that $\overline{CAS}$ will not begin to go inactive until a minimum of {} ns after $\overline{RAS}$ has gone active in a refresh cycle. 4)	185	–	230	–	307	–	ns
t_{49}	Guarantees that $\overline{RAS}$ will not begin to go active until a minimum of {} ns after $\overline{XF/G}$ is active in a transfer cycle. 4)	12	–	13	–	21.5	–	ns
t_{50}	Guarantees that the start offset on CDAT will be valid and stable for a minimum of {} ns before $\overline{RAS}$ begins to go active in a transfer cycle. 4)	10	–	11	–	21.5	–	ns
t_{51}	Guarantees that the start offset on CDAT will remain valid and stable for a minimum of {} ns after $\overline{RAS}$ has gone active in a transfer cycle. 4)	65	–	78	–	104.5	–	ns

For notes refer to page 374.

Display Memory Interface Timing (cont'd)

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{52}	Guarantees that VSTB will be high for a minimum of {} ns before $\overline{RAS}$ begins to go active in a transfer cycle. 4)	90	–	109	–	146	–	ns
t_{53}	Guarantees that VSTB will remain high for a minimum of {} ns after $\overline{RAS}$ has gone inactive in a transfer cycle. 4)	40	–	47	–	63	–	ns
t_{54}	Guarantees that DSTB will be low for a minimum of {} ns before $\overline{RAS}$ begins to go active in a transfer cycle. 4)	90	–	109	–	146	–	ns
t_{55}	Guarantees that DSTB will remain low for a minimum of {} ns after $\overline{RAS}$ has gone inactive in a transfer cycle.	40	–	47	–	63	–	ns
t_{56}	Guarantees that $\overline{CAS}$ will not become active until a minimum of {} ns after $\overline{RAS}$ has gone active. This is for a write cycle. See parameter t_{36} for read and transfer cycles. 4)	90	–	109	–	140	–	ns
t_{57}	Guarantees that $\overline{CAS}$ will be active for a minimum of {} ns for a write cycle. See parameter t_{39} for read and transfer cycles. 4)	80	–	100	–	146	–	ns
t_{58}	Guarantees that $\overline{WE0}$-$\overline{WE3}$ will be active for a minimum of {} ns in the case of a masked write. 4)	180	–	225	–	312	–	ns
t_{59}	Guarantees that $\overline{WE0}$-$\overline{WE3}$ will be active for a minimum of {} ns before $\overline{RAS}$ begins to fall in the case of a masked write. 4) 5)	11	–	14	–	21.5	–	ns
t_{60}	Guarantees that $\overline{WE0}$-$\overline{WE3}$ will be active for a minimum of {} ns before $\overline{CAS}$ begins to fall in the case of an unmasked write. 4)	13	–	14	–	21.5	–	ns
t_{61}	Guarantees that $\overline{WE0}$-$\overline{WE3}$ will be active for a minimum of {} ns in the case of an unmasked write. 4)	78	–	100	–	140	–	ns

For notes refer to page 34

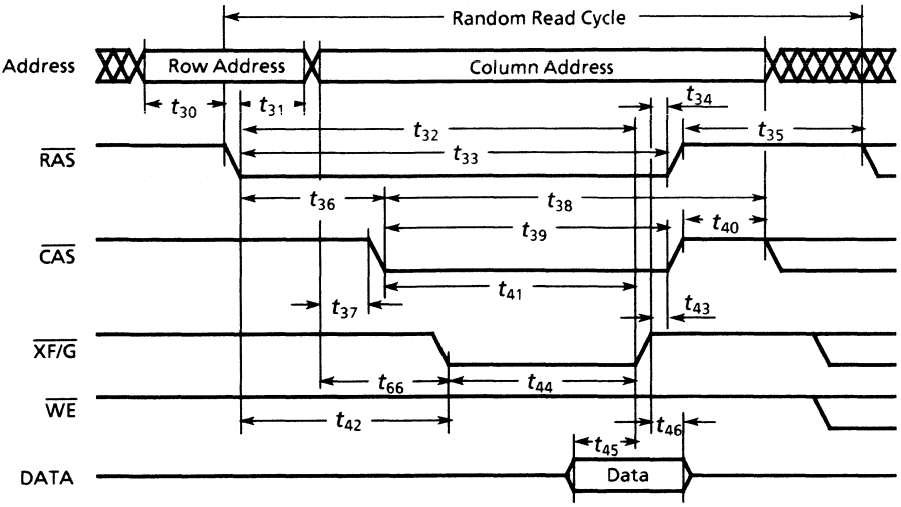
Display Memory Interface Timing (cont'd)

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{62}	Guarantees that the write mask will be valid and stable on the DM pins {} ns before $\overline{RAS}$ begins to go active.	2	–	7	–	15	–	ns
t_{63}	Guarantees that the write mask will remain active {} ns after $\overline{RAS}$ has gone active. 4)	60	–	73	–	104.5	–	ns
t_{64}	Guarantees that the write data will be valid and stable on the DM pins {} ns before $\overline{CAS}$ begins to go active.	2	–	7	–	15	–	ns
t_{65}	Guarantees that the write data will remain active {} ns after $\overline{CAS}$ has gone active. 4)	60	–	73	–	104.5	–	ns
t_{66}	Guarantees that the column address will be valid {} ns before $\overline{XF/G}$ goes active.	–8	–	–12	–	–16	–	ns

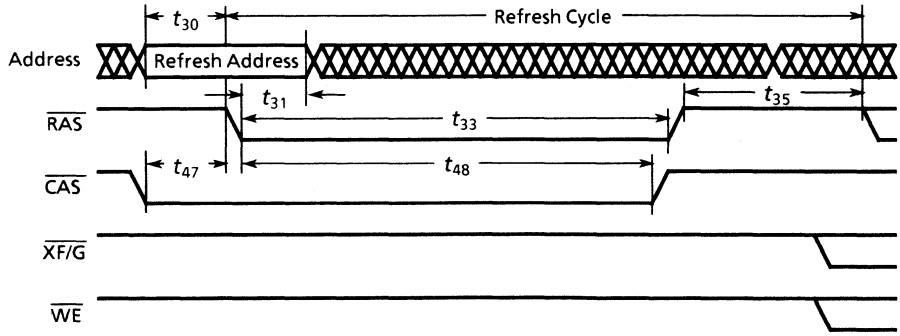
For notes refer to page 374.

Display Memory Interface Timing Waveforms

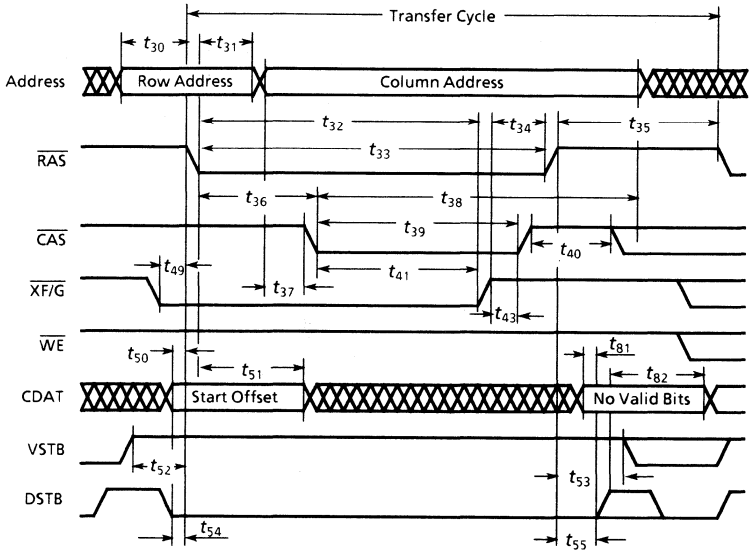
Display Memory Read Cycle



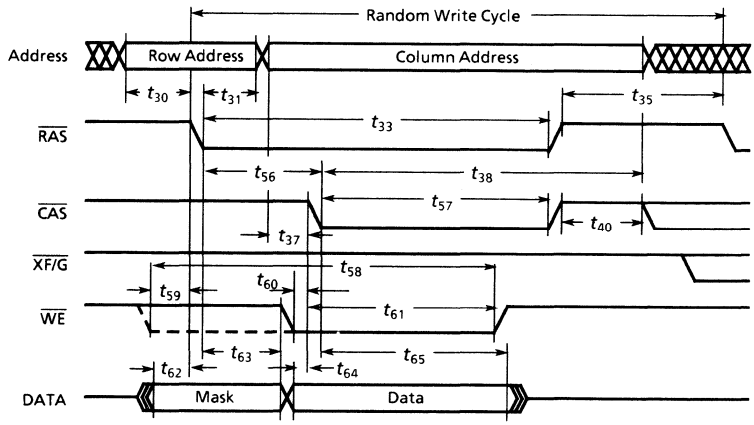
Display Memory Dynamic RAM Refresh Cycle



Display Memory Transfer Cycle



Display Memory Write Cycle



AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 5%

VDAF Interface Timing

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{80}	Guarantees that VSTB will change to the new state within 0-{} ns following the positive edge of DSTB.	0	10	0	10	0	10	ns
t_{81}	Guarantees that the value on CDAT will be valid and stable for a minimum of {} ns before DSTB begins to rise.	0	–	0	–	5	–	ns
t_{82}	Guarantees that the value on CDAT will remain valid for a minimum of {} ns after the rising edge of DSTB.	20	–	30	–	40	–	ns
t_{83}	Guarantees that the positive edges on DSTB will occur with the same period as SYSCLK. 4)	50	–	62	–	83	–	ns
t_{84}	Guarantees that $\overline{\text{FULL}}$ will be recognized at the current SYSCLK cycle if it is valid for a minimum of {} ns before the edge. This is not an operating parameter; if this setup time is not met, the part will not go metastable.	–	25	–	50	–	75	ns
t_{85}	Requires that $\overline{\text{FULL}}$ remains active for at least one SYSCLK period. 4)	50	–	62	–	83	–	ns
t_{86}	Guarantees that a positive edge will not occur on DSTB until a minimum of {} ns following $\overline{\text{FULL}}$ going inactive. 4)	150	–	186	–	249	–	ns

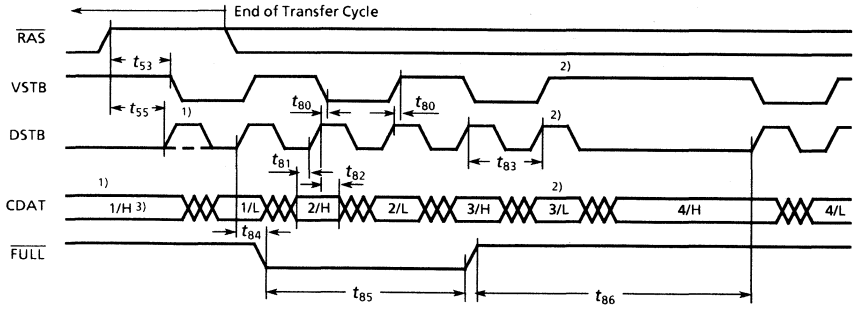
Memory Bus Arbitration Timing

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{90}	Guarantees that the SAB 95C60 will set $\overline{\text{MEMAVL}}$ inactive within {} ns of $\overline{\text{MEMREQ}}$ going inactive. 4)	–	160	–	190	–	245.5	ns
t_{91}	Guarantees that the SAB 95C60 will not begin a memory cycle for a minimum of {} ns following the rising edge of $\overline{\text{MEMAVL}}$. 4) 6)	450	–	558	–	747	–	ns

For notes refer to page 374.

VDAF Interface Timing Waveforms

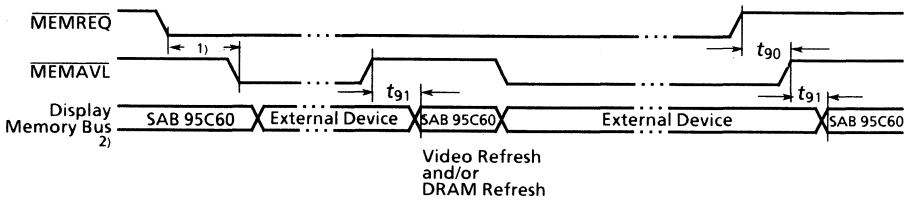
VDAF Interface



1) DSTB and CDAT for (1/H) only occurs on even boundaries.
2) One less byte may be strobed after $\overline{\text{FULL}}$ active.
3) CDAT 1/H = CDAT for 1st word high byte.

Memory Bus Arbitration Timing Waveforms

Display Memory Arbitration



1) $\overline{\text{MEMREQ}}$ to $\overline{\text{MEMAVL}}$ delay = Minimum 6 CLKs for arbitration cycle
= Maximum 12 CLKs if DRAM refresh lower priority
= Maximum 18 CLKs DRAM refresh higher priority
} Not an operating parameter provided for reference only

2) Display memory bus = $\overline{\text{ADDR}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{XF/G}}$, WE, DATA
t_{91} is referred to $\overline{\text{RAS}}$ falling edge, which defines the start of the QPDM cycle

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5%

Miscellaneous Timings

Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{100}	Guarantees that transitions on $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ will occur for a maximum of {} ns following the high-to-low transition of VIDCLK. This applies only if $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ are programmed as output(s).	–	25	–	31	–	41	ns
t_{101}	Requires that $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ are valid for a minimum of {} ns prior to the rising edge of CIDCLK. This is not an operational parameter. If this setup time is not met, the SAB 95C60 will not become metastable.	0	–	0	–	0	–	ns
t_{102}	Requires that $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ remain valid for a minimum of {} ns after VIDCLK has fallen low. This is not an operational parameter. If this hold time is not met, the SAB 95C60 will not become metastable.	15	–	20	–	25	–	ns
t_{103}	Guarantees that transitions on BLANK, HSYNC and VSYNC will occur within a maximum of {} ns after the rising edge of VIDCLK.	–	30	–	40	–	50	ns
t_{104}	Requires that VODD/$\overline{\text{EVEN}}$ is valid for a minimum of {} ns prior to the rising edge of VIDCLK.	15	–	20	–	25	–	ns
t_{105}	Requires that VODD/$\overline{\text{EVEN}}$ remain valid for a minimum of {} ns after VIDCLK has risen high.	15	–	20	–	25	–	ns
t_{106}	Requires that the period of SYSCLK lies between {} and {} ns.	50	500	62	500	83	500	ns
t_{107}	Requires that SYSCLK transition times lie within a maximum of {} ns.	–	5	–	5	–	5	ns
t_{108}	Requires that the SYSCLK low time is a minimum of {} ns.	18	–	23	–	32	–	ns
t_{109}	Requires that the SYSCLK high time is a minimum of {} ns.	18	–	23	–	32	–	ns

Miscellaneous Timings (cont'd)

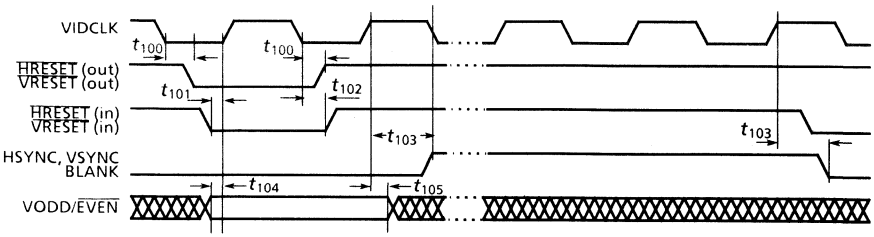
Symbol	Parameter	Limit values						Unit
		20 MHz		16 MHz		12 MHz		
		min.	max.	min.	max.	min.	max.	
t_{110}	Requires that the period of VIDCLK is minimum of {} ns and a maximum of {} µs.	66	4 µs	72	4 µs	83	4 µs	ns
t_{111}	Requires that the VIDCLK transition times are a maximum of {} ns.	–	5	–	5	–	5	ns
t_{112}	Requires that the VIDCLK low time is a minimum of {} ns.	25	–	27	–	32	–	ns
t_{113}	Requires that the VIDCLK high time is a minimum of {} ns.	25	–	27	–	32	–	ns
t_{114}	Requires that $\overline{\text{RESET}}$ remains active for a minimum of {} ns. 4)	200	–	248	–	332	–	ns
t_{115}	Requires that the external delay from TSYNOUT to TSYNIN and the external delay from MATOUT to MATIN is a maximum of {} ns.	–	20	–	25	–	30	ns

Notes:

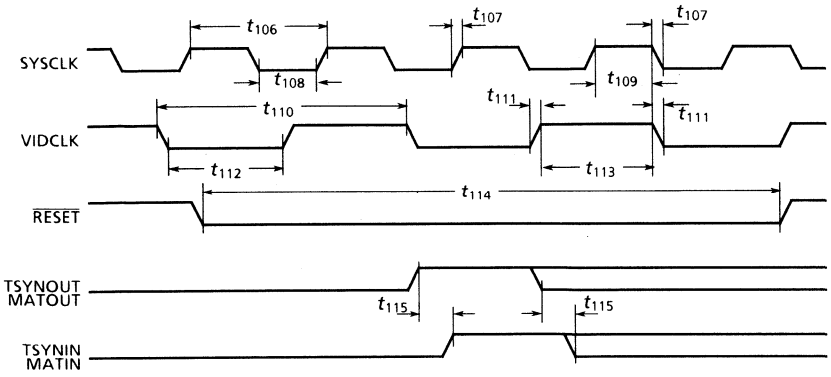
1) Timings are referred to $\overline{\text{CS}}$ or $\overline{\text{ACKD}}$.
2) $\overline{\text{RD}}$ and $\overline{\text{WR}}$ reverse operations in fly-by DMA cycles.
3) Timings are referred to $\overline{\text{RD}}$/$\overline{\text{WR}}$ or $\overline{\text{ACKD}}$ rising edge, whichever occurs first.
4) Require a SYSCLK symmetry of no worse than 45/55%.
5) This timing applies to masked writes.
6) All display memory cycles are exactly six SYSCLK cycles.

Miscellaneous Waveforms

Video Control



Clocks, Reset and SAB 95C60 Synchronization



Ordering Information

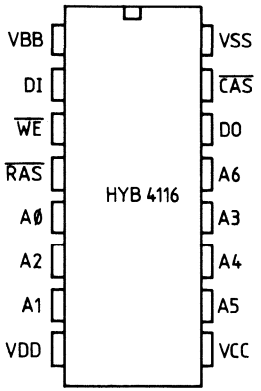
Type	Ordering code	Description
SAB 95C60-12-A	Q67120-P267	Quad pixel dataflow manager (QPDM)
SAB 95C60-16-A	Q67120-P268	Quad pixel dataflow manager (QPDM)
SAB 95C60-20-A	Q67120-P269	Quad pixel dataflow manger (QPDM)

Memories

HYB 4116-2, HYB 4116-3
16,384-Bit Dynamic Random Access Memory (RAM)

- Fully decoded, 16,384 X1 bit organization
- Separate data input and output
- All inputs including clocks TTL compatible
- Low power dissipation
  462 mW active, 20 mW standby
  150 ns access time,
  320 ns cycle time (HYB 4116-P2)
  200 ns access time,
  375 ns cycle time (HYB 4116-P3)
- Three-state output, 2 TTL loads
- Compatible with MK 4116
- 128 refresh cycles
- Data output is unlatched

Pin Configuration



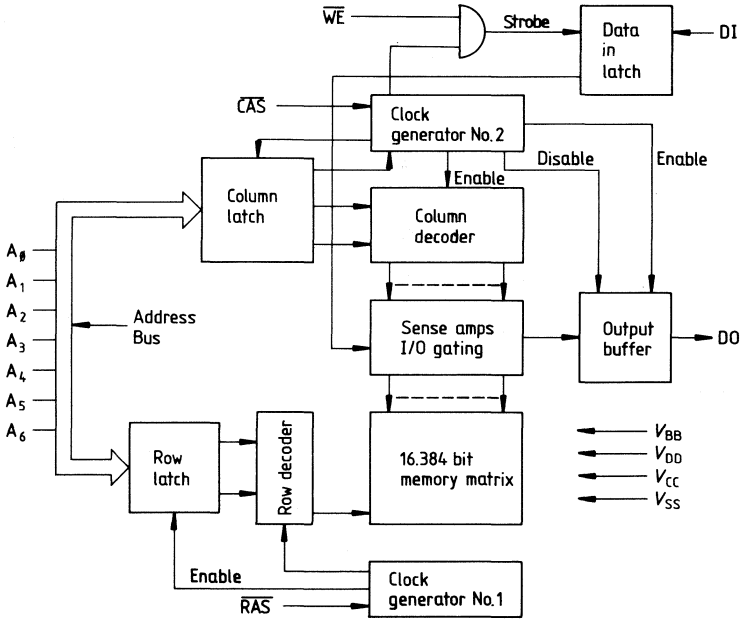
Pin Names

A0 – A6	Address inputs
$\overline{CAS}$	Column address strobe
DI	Data in
DO	Data out
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/write input
V_{BB}	Power supply (−5 V)
V_{CC}	Power supply (+5 V)
V_{DD}	Power supply (+12 V)
V_{SS}	Ground (0 V)

The HYB 4116 manufactured by Siemens is a dynamic random access memory built in N-channel silicon gate technology, using double layer polysilicon.

The dynamic one-transistor cell ensures high packing density and high speed. Moreover, multiplexing of the address signals permits the use of the space-saving 16-pin dual in-line package.

Block Diagram



Functional Description

Addressing (A0–A6)

For selecting one of the 16,384 memory cells, a total of 14 address bits is required which is consecutively applied via pins A0 to A6 by means of two strobes (address multiplexing). First the seven row addresses are called up and accepted with strobe $\overline{RAS}$ into the row select buffer. Following this, the seven column addresses are deposited in the column select buffer with $\overline{CAS}$. It should be noted that the address signals are available in their steady-state condition at the time of the negative pulse edge of $\overline{RAS}$ and $\overline{CAS}$, respectively.
$\overline{RAS}$ and $\overline{CAS}$ determine the starting point of the internal clock control.
$\overline{RAS}$ initiates row decoding and activates the read amplifier. $\overline{CAS}$ controls column decoding as well as the data input and output amplifiers.

Read write ($\overline{WE}$)

Read and write operations are executed when the write enable signal $\overline{WE}$ is at "H" or "L". Data input DI is disabled as long as reading takes place.
The shortest write cycle time is obtained when $\overline{WE}$ goes to logic "L" ahead of or simultaneously with $\overline{CAS}$ ("early write"). The write data is then accepted into the input data memory by means of $\overline{CAS}$.

Delayed writing, read-modify-write

If writing or read-modify-write is delayed, $\overline{CAS}$ is already at logic "L" so that the write data is transferred to the input data memory with the subsequent $\overline{WE}$ signal.

Data input (DI)

Data can be input during a write or a read-modify-write cycle. The strobe for the data input is the last one of signals $\overline{WE}$ or $\overline{CAS}$ to make its negative transition.

Data output (DO)

The data output may assume three states (Tri-state logic) and is rated for driving two TTL loads. As against the output data the input data is not inverted.
In a read cycle the read data is available after access time tCAC referred to $\overline{CAS}$. At the end of the read cycle, when $\overline{CAS}$ is again "H", the data output assumes again the high impedance condition.
In the case of read-modify-write the data output contains the data read from the selected cell as in the read cycle. For "early write" the output pin assumes a high impedance troughout the entire cycle.

Refresh cycle

To prevent data in the dynamic memory cells from getting lost, each row address must be called up at least every two milliseconds. A total of 128 refresh cycles must be executed for all row addresses during this 2 millisecond period.
During writing or reading the data in the 128 memory cells of a row-line is automatically refreshed.

Precharge cycle

After power is applied to the device, the HYB 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

Absolute Maximum Ratings *)

Operating Temperature Range	0 to 70 °C
Storage Temperature Range	−65 to 150 °C
Voltage on any pin relative to V_{BB}	−0.5 to 20 V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	−1 to 15 V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} \geqq 0$ V)	0 V
Power Dissipation	1 W

D.C. Characteristics [1]

T_A = 0 to 70 °C; V_{SS} = 0 V, V_{DD} = +12 V ±10%, V_{BB} = −5 V ±10%, V_{CC} = +5 V ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IH}	High level input voltage, (all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$) [2]	2.4	7.0	V	–
V_{IHC}	High level input voltage ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$) [2]	2.4	7.0		
V_{IL}	Low level input voltage [2]	−1.0	0.8		
V_{OH}	Output high voltage	2.4	V_{CC}		I_O = −5 mA
V_{OL}	Output low voltage	–	0.4		I_O = 4.2 mA
I_{DD1}	Average V_{DD} supply current [3]	–	35	mA	–
I_{DD2}	Standby V_{DD} supply current	–	1.5		$\overline{RAS}$ at V_{IH} $\overline{CAS}$ at V_{IH}
I_{DD3}	Average V_{DD} current during refresh [3]	–	27		$\overline{RAS}$ cycling $\overline{CAS}$ at V_{IH}
$I_{I(L)}$	Input leakage current (any input) [4]	−10	10	µA	–
$I_{O(L)}$	Output leakage current	−10	10		$\overline{CAS}$ at V_{IH} $V_O = V_{SS}$ to V_{CC}
I_{CC}	V_{CC} supply current [5]	−10	10		$\overline{CAS}$ at V_{IH} $\overline{RAS}$ at V_{IH}
I_{BB1}	Average V_{BB} power supply current	–	200		–
I_{BB2}	Standby V_{BB} power supply current	–	100		

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
C_{I1}	Input capacitance [6] (A_0–A_6), DI	–	5	pF	–
C_{I2}	Input capacitance [6] $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	–	10		
C_O	Output capacitance [6]	–	7		DO disabled

1) The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC} and V_{SS} should never be 0.3 V more negative than V_{BB}.
2) Over- and undershooting on input levels of 6.5 V or −2 V for a period of 30 ns will not influence function and reliability of the device.
3) I_{DD} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.
4) All device pins at 0 V except V_{BB} at −5 V and pin under test which is at +7 V.
5) V_{CC} is connected to output buffer only.
6) Effective capacitance calculated from the equation
$C = \frac{I \cdot \Delta t}{\Delta V}$ with $\Delta V = 3$ V.

A.C. Characteristics [1]

T_A = 0 to +70 °C; V_{SS} = 0V; V_{DD} = 12V ±10%; V_{BB} = −5V ±10%; V_{CC} = +5V ±10%

Symbol	Parameter	Limit Values				Units
		HYB 4116–P2		HYB 4116–P3		
		Min.	Max.	Min.	Max.	
t_{RC}	Random read or write cycle time [2]	320	–	375	–	ns
t_{RWC}	Read/write cycle time [2]	320	–	375	–	
t_{RMWC}	Read/modify/write cycle time [2]	320	–	405	–	
t_{RAC}	Access time from $\overline{RAS}$ [3] [4]	–	150	–	200	
t_{CAC}	Access time from $\overline{CAS}$ [3] [5]	–	100	–	135	
t_{OFF}	Output buffer turn-off delay [6]	–	40	0	50	
t_{RP}	$\overline{RAS}$ precharge time	100	–	120	–	
t_{RAS}	$\overline{RAS}$ pulse width	150	10^4	200	10^4	
t_{RSH}	$\overline{RAS}$ hold time	100	–	135	–	
t_{CSH}	$\overline{CAS}$ hold time	150	–	200	–	
t_{CAS}	$\overline{CAS}$ pulse width	100	–	135	–	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [7]	20	50	25	65	
t_{ASR}	Row address set-up time	0	–	0	–	
t_{RAH}	Row address hold time	20	–	25	–	
t_{ASC}	Column address set-up time	−5	–	−10	–	
t_{CAH}	Column address hold time	45	–	55	–	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95	–	120	–	
t_T	Transition time (rise and fall)	3	35	3	50	
t_{RCS}	Read command set-up time (RMW)	0	–	0	–	
t_{RCH}	Read command hold time	0	–	0	–	
t_{WCH}	Write command hold time	45	–	55	–	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95	–	120	–	
t_{WCS}	Write command set-up time [8]	−20	–	−20	–	

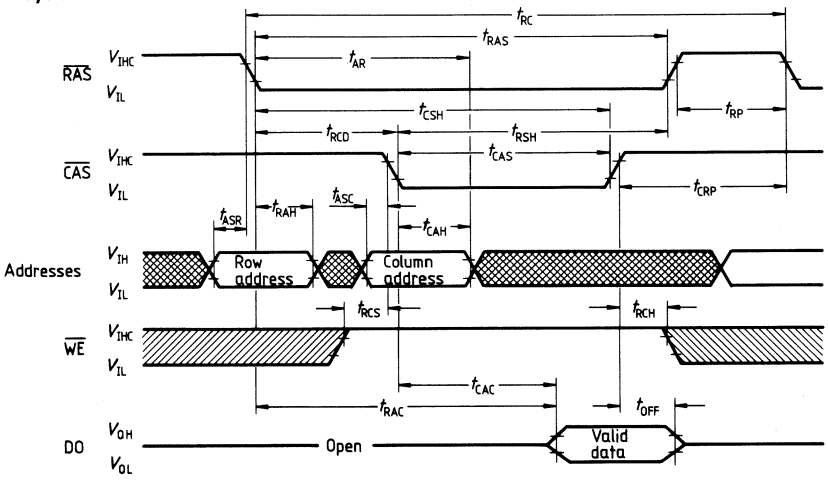
Symbol	Parameter	Limit Values				Units
		HYB 4116–P2		HYB 4116–P3		
		Min.	Max.	Min.	Max.	
t_{WP}	Write command pulse width	45	–	55	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	50	–	70	–	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50	–	70	–	
t_{DS}	Data in set-up time	0	–	0	–	
t_{DH}	Data in hold time [9]	45	–	55	–	
t_{DHR}	Data in hold time [9] referenced to $\overline{RAS}$	95	–	120	–	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	−20	–	−20	–	
t_{RF}	Refresh period	–	2.0	–	2.0	ms
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay [8]	60	–	95	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay [8]	110	–	160	–	

Notes:

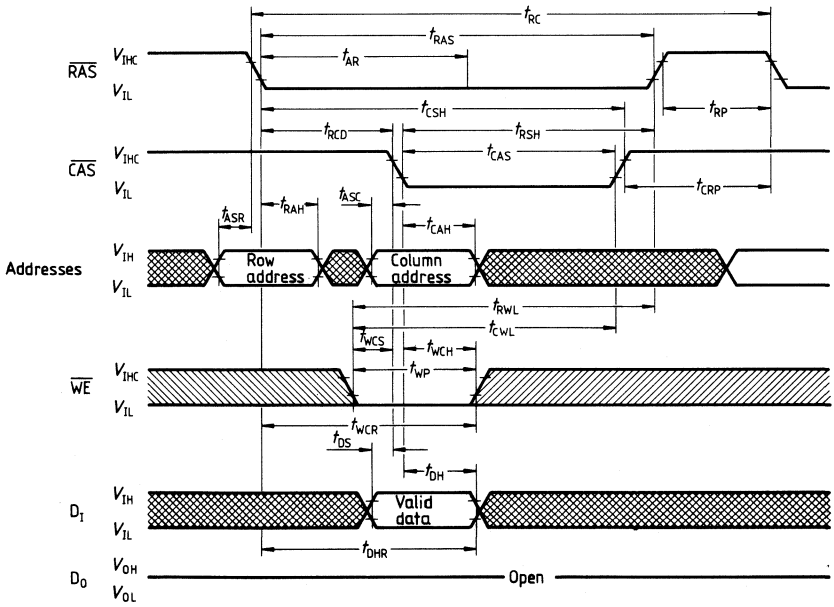
1) $V_{IHC\,(min)}$ or $V_{IH\,(min)}$ and $V_{IL\,(min)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
2) The specifications for $t_{RC\,(min)}$ and $t_{RWC\,(min)}$ are used only to indicate cycle time at which proper operation over full temperature range ($0\,°C \leq T_A \leq 70\,°C$) is assured.
3) Measured with a load equivalent to two TTL loads and 100 pF.
4) Assumes that $t_{RCD} \leq t_{RCD\,(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} \geq t_{RCD\,(max)}$.
6) $t_{OFF\,(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7) Operation within the $t_{RCD\,(max)}$ limit ensures that $t_{RAC\,(max)}$ can be met. $t_{RCD\,(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD\,(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{CWS\,(min)}$, the cycle is an early write cycle and the data-out pin will remain open circuit (high impedance) throughout the entire cycle: if $t_{CWD} \geq t_{CWD\,(min)}$ and $t_{RWD} \geq t_{RWD\,(min)}$ the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9) t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

Waveforms

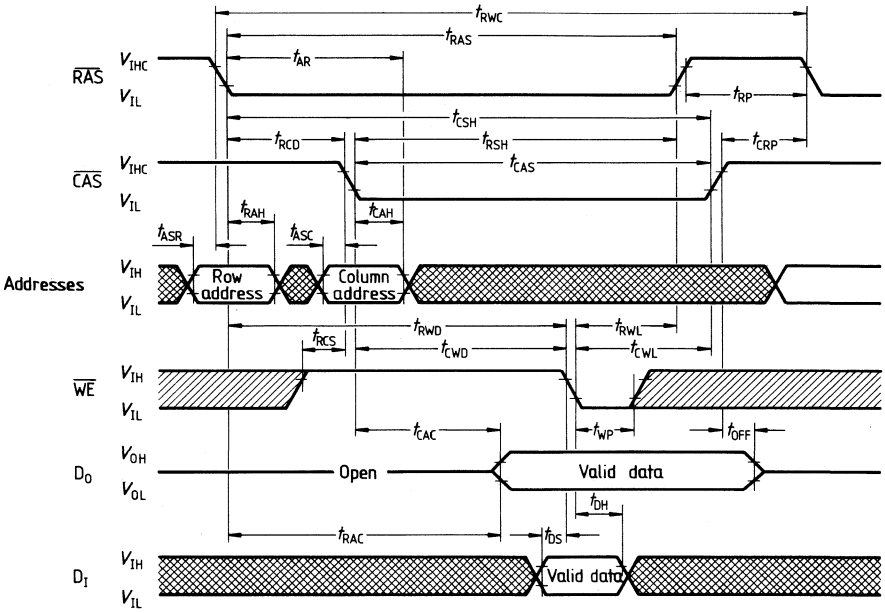
Read cycle



Write cycle (early write)

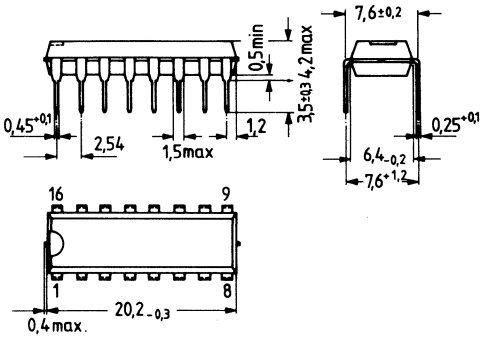


Read-write/read-modify-write cycle



Package Outline

16 Pin Plastic Package Type P



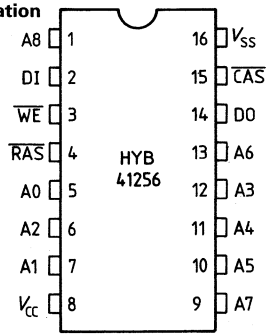
Ordering Information

Type	Description	Ordering Code
HYB 4116-P 2	RAM (Plastic; 150 ns)	Q 67100-Q 308
HYB 4116-P 3	RAM (Plastic; 200 ns)	Q 67100-Q 306

HYB 41256-10/-12/-15
262,144-Bit Dynamic RAM

- 262,144 × 1-bit organization
- Industry standard 16 pins
- Single +5 V supply, ±10% tolerance
- Low power dissipation:
  - 358 mW active (max.)
  - 28 mW standby (max.)
- 100 ns access time
  200 ns cycle time (HYB 41256-10)
  120 ns access time
  220 ns cycle time (HYB 41256-12)
  150 ns access time
  260 ns cycle time (HYB 41256-15)
- All inputs and outputs TTL- compatible
- On-chip substrate bias generator
- Tristate data output
- Read, write, read-modify-write, $\overline{RAS}$-only refresh, hidden refresh
- Common I/O capability using "early write" operation
- Page mode read and write, read-write
- 256 refresh cycles with 4 ms refresh period
- Redundancy incorporated for increasing yield – activation via laser links

Pin Configuration



Pin Names

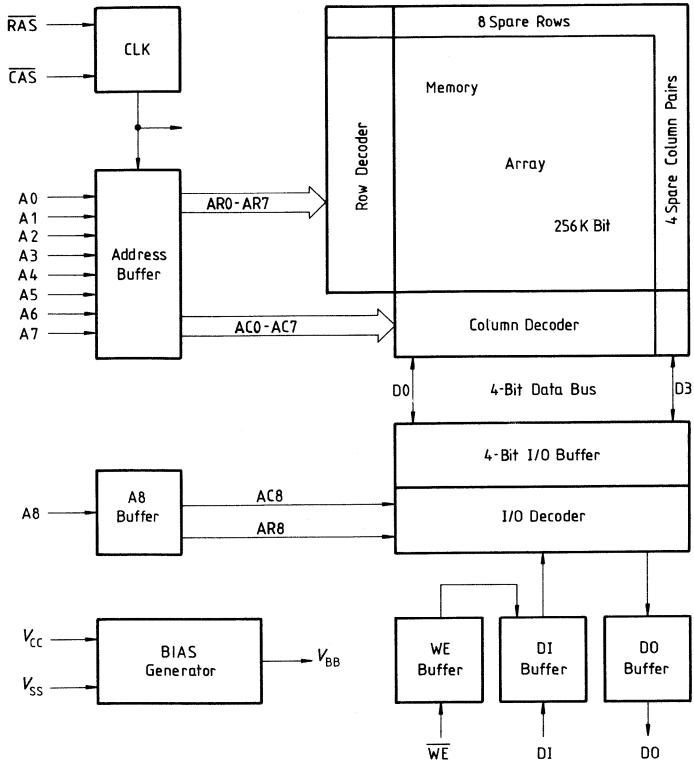
A0 – A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DI	Data Input
DO	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground (0 V)

The HYB 41256 is a 262,144 word by 1-bit dynamic random access memory. This 5V-only component is fabricated with Siemens high-performance N-channel silicon gate technology. The use of tantalum polycide provides high speed. A low radiation molding compound protects the chip against soft errors.
Nine multiplexed address inputs permit the HYB 41256 to be packaged in an industry standard 16-pin dual-in-line package. System-oriented features include single power supply with ±10% tolerance, on-chip address and data registers which eliminate the need for interface registers, and fully TTL-compatible inputs and output, including clocks.

In addition to the usual read, write and read-modify-write cycles, the HYB 41256 is capable of early and late write cycles, $\overline{RAS}$-only refresh, and hidden refresh. Common I/O capability is given by using early write operation.
The HYB 41256 also features page mode which allows high-speed random access of bits in the same row.
The HYB 41256 has the capability of using laser links to perform redundancy.

9.87

Block Diagram



Functional Description

Device Initialization

Since the HYB 41256 is a dynamic RAM with a single 5 V supply, no power sequencing is required. For power-up, an initial pause of 200 microseconds is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the row address strobe ($\overline{RAS}$) has to be performed. This is also necessary after an extended inactive state of greater than 4 milliseconds.

Adressing (A0 – A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits is required. First, 9 row address bits are set up on pins A0 through A8 and latched into the row address latches by the row address strobe ($\overline{RAS}$). Then, the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the column address strobe ($\overline{CAS}$). All input addresses must be stable on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. It should be noted that $\overline{RAS}$ is similar to a "chip enable" insofar as it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

Write Enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (V_{IH}) on $\overline{WE}$ dictates read mode; logic low (V_{IL}) dictates write mode. The data input is disabled when read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data Output (DO)

The output is tristate TTL-compatible with a fan-out of two standard TTL loads. DO has the same polarity as DI. The output is in a high-impedance state until $\overline{CAS}$ is brought low. In a read cycle or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (min.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. With $\overline{CAS}$ going high the output returns to the high-impedance state within t_{OFF}.

Hidden refresh

$\overline{RAS}$-only refresh cycle may take place while maintaining valid output data. This feature is referred to as hidden refresh. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} of a previous memory read cycle.

Refresh cycle

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$, causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Page mode

Page-mode operation allows effectively faster memory access by maintaining the row address and strobing random column addresses on the chip. Thus, the time necessary to setup and strobe sequential row addresses for the same page is no longer required. The maximum number of columns that can be addressed in sequence is determined by t_{RAS}, the maximum $\overline{RAS}$ low pulse width.

Absolute Maximum Ratings[1)]

Operating temperature range	0 to 70 °C
Storage temperature range	−65 to 150 °C
Voltage on any pin relative to V_{SS}	−1 to 7 V
Power dissipation	1 W
Data output current (short circuit)	50 mA

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = +5 V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage (all inputs)	2.4	V_{CC}+1	V	2) 3)
V_{IL}	Input low voltage (all inputs)	−1.0	0.8	V	2) 3)
V_{OH}	Output high voltage	2.4	–	V	7)
V_{OL}	Output low voltage	–	0.4	V	8)
I_{CC1}	Average V_{CC} supply current −10 t_{RC} = 200 ns −12 t_{RC} = 220 ns −15 t_{RC} = 260 ns	 –	 85 75 65	 mA	4)
I_{CC2}	Standby V_{CC} supply current	–	5	mA	5)
I_{CC3}	Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles −10 t_{RC} = 200 ns −12 t_{RC} = 220 ns −15 t_{RC} = 260 ns	 –	 70 60 50	 mA	4)
I_{CC4}	Average V_{CC} supply current during page mode −10 t_{PC} = 100 ns −12 t_{PC} = 120 ns −15 t_{PC} = 150 ns	 –	 70 60 50	 mA	4)
$I_{I(L)}$	Input leakage current (any input)	−10	10	µA	–
$I_{O(L)}$	Output leakage current ($\overline{CAS}$ at logic 1, 0 ≤ Vout ≤ 5.5)	−10	10	µA	–
V_{CC}	V_{CC} supply voltage	4.5	5.5	V	2)
V_{SS}	V_{SS} supply voltage	0	0	V	2)

Notes see next page.

Capacitance

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{I1}	Input capacitance (A0–A8, DI)	–	5	pF	6)
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	–	7	pF	6)
C_O	Output capacitance (DO, $\overline{CAS} = V_{IH}$ to disable output)	–	7	pF	6)

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) All voltages refered to V_{SS}.

3) Overshooting and undershooting on input levels of 6.5 V or −2 V for a period of 30 ns max. will not influence function and reliability of the device.

4) I_{CC} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

5) $\overline{RAS}$ and $\overline{CAS}$ are both at V_{IH}.

6) Effective capacitance calculated from the equation. $C = \frac{I \cdot \triangle t}{\triangle V}$ with $\triangle V = 3$ V or measured with Boonton meter.

7) $I_{OH} = -5.0$ mA

8) $I_{OL} = +4.2$ mA

AC Test Conditions

Input pulse levels		0 to 3.0 V
Input rise and fall times	5 ns between	0.8 and 2.4 V
Input timing reference levels		0.8 to 2.4 V
Output timing reference levels		0.4 to 2.4 V
Output load		equivalent to 2 standard TTL loads and 100 pF

AC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5 V ±10% (unless otherwise specified; see notes 9, 10, 11)

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		−10		−12		−15		
		min.	max.	min.	max.	min.	max.	
t_{RC}	Random read or write cycle time [12]	200	–	220	–	260	–	ns
t_{RWC}	Read-modify-write cycle time [12]	235	–	265	–	310	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [13] [14]	–	100	–	120	–	150	ns
t_{CAC}	Access time from $\overline{CAS}$ [13] [15]	–	50	–	60	–	75	ns
t_{RAS}	$\overline{RAS}$ pulse width	100	10^4	120	10^4	150	10^4	ns
t_{CAS}	$\overline{CAS}$ pulse width	50	–	60	–	75	–	ns
t_{REF}	Refresh period	–	4	–	4	–	4	ms
t_{RP}	$\overline{RAS}$ precharge time	90	–	90	–	100	–	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0	–	0	–	0	–	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [16]	25	50	30	60	30	75	ns
t_{RSH}	$\overline{RAS}$ hold time	50	–	60	–	75	–	ns
t_{CSH}	$\overline{CAS}$ hold time	100	–	120	–	150	–	ns
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns
t_{RAH}	Row address hold time	15	–	20	–	20	–	ns
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns
t_{CAH}	Column address hold time	20	–	30	–	30	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$ [17]	70	–	90	–	105	–	ns
t_T	Transition time (rise and fall) [9]	3	50	3	50	3	50	ns
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns
t_{RCH}	Read command hold time referenced to $\overline{CAS}$ [18]	0	–	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [18]	10	–	10	–	10	–	ns
t_{OFF}	Output buffer turn-off delay [19]	0	30	0	30	0	40	ns
t_{WCS}	Write command setup time [20]	0	–	0	–	0	–	ns
t_{WCH}	Write command hold time	35	–	40	–	45	–	ns

Notes see next page.

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		−10		−12		−15		
		min.	max.	min.	max.	min.	max.	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$ [17]	100	–	100	–	120	–	ns
t_{WP}	Write command pulse width	30	–	40	–	45	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	30	–	40		45	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	30	–	40	–	45	–	ns
t_{DS}	Data in setup time [21]	0	–	0	–	0	–	ns
t_{DH}	Data in hold time [21]	30	–	40	–	45	–	ns
t_{DHR}	Data in hold time referenced to $\overline{RAS}$ [17]	90	–	100	–	120	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay [20]	50	–	60	–	75	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay [20]	100	–	120	–	150	–	ns
t_{RRW}	RMW cycle $\overline{RAS}$ pulse width	140	–	165	–	200	–	ns
t_{CRW}	RMW cycle $\overline{CAS}$ pulse width	85	–	105	–	125	–	ns
t_{PC}	Page mode cycle time [12]	100	–	120	–	145	–	ns
t_{PRWC}	Page mode read-write cycle time	130	–	160	–	190	–	ns
t_{CP}	Page mode $\overline{CAS}$ precharge time	40	–	50	–	60	–	ns

9) V_{IH} and V_{IL} are reference levels to measure timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10) An initial pause of 200 µs is required after power-up followed by a minimum of eight initialization cycles prior to normal operation.

11) The time parameters specified here are valid for a transition time of $t_T = 5$ ns for the input signals.

12) The specification for t_{RC} (min.), t_{RWC} (min.), and page-mode cycle time (t_{PC}) are only used to indicate cycle time at which proper operation over full temperature range (0 °C ≤ T_A ≤ 70 °C) is assured.

13) Measured with a load equivalent to two TTL loads and 100 pF.

14) Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

15) Assumes that $t_{RCD} \geq t_{RCD}$ (max.).

16) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

17) $t_{RCD} + t_{CAH} \geq t_{AR}$ min., $t_{RCD} + t_{DH} \geq t_{DHR}$ min., $t_{RCD} + t_{WCH} \geq t_{WCR}$ min.

18) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

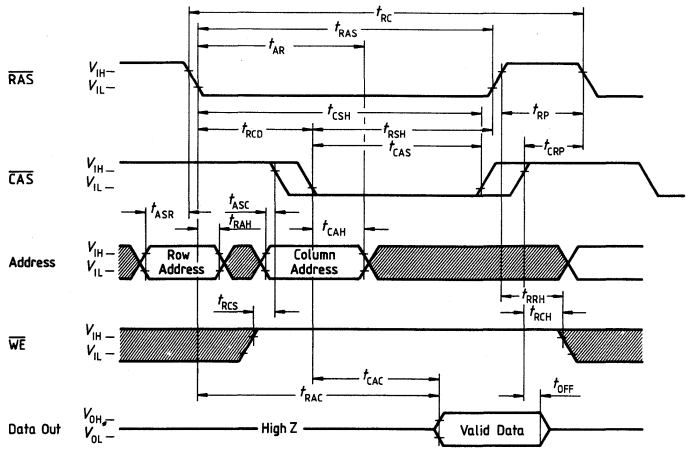
19) t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

20) t_{WCS}, t_{CWD} and t_{RWC} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open-circuit (high-impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.) the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.

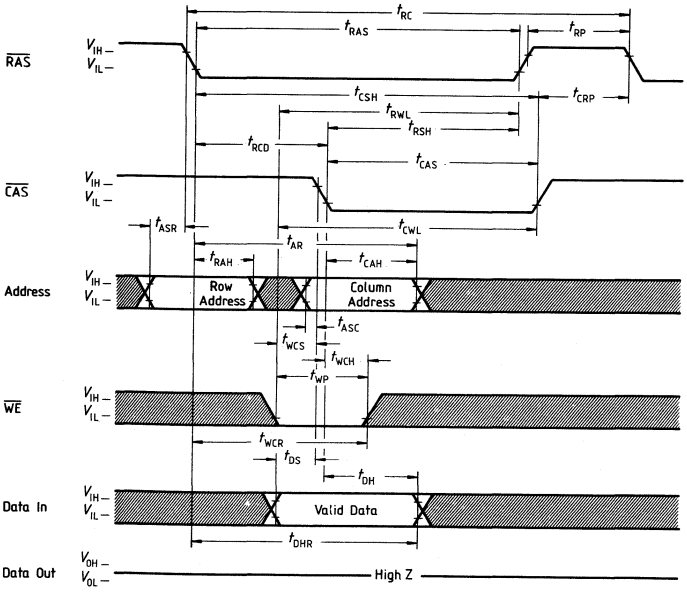
21) t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write of read-modify-write cycles.

Waveforms

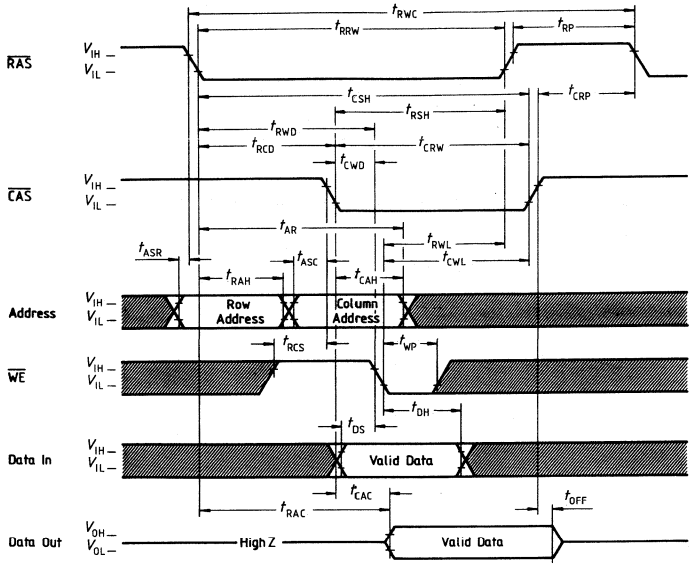
Read Cycle



Write Cycle (early write)

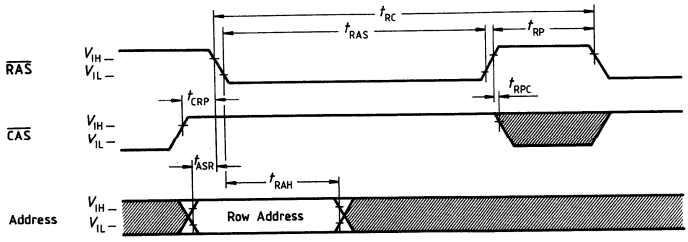


Read-Modify-Write or Late Write Cycle

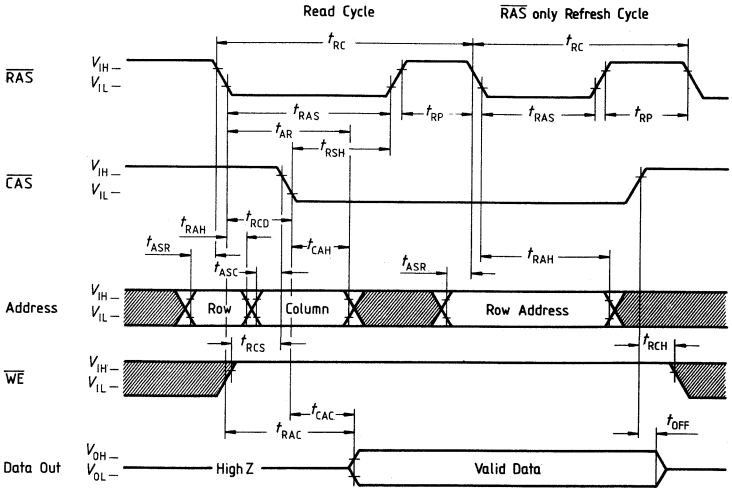


$\overline{RAS}$-Only Refresh Cycle

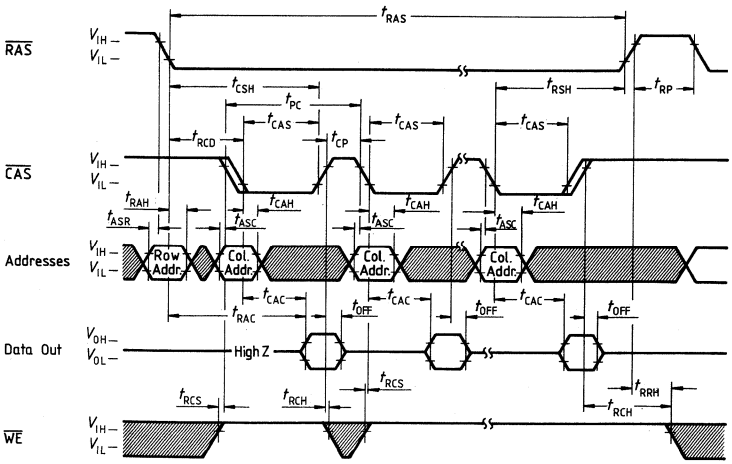
(DI and $\overline{WE}$ = don't care)



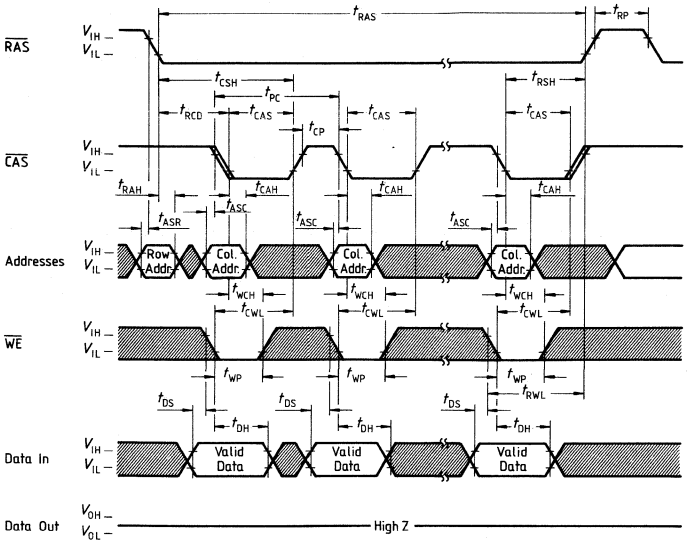
Hidden Refresh Cycle



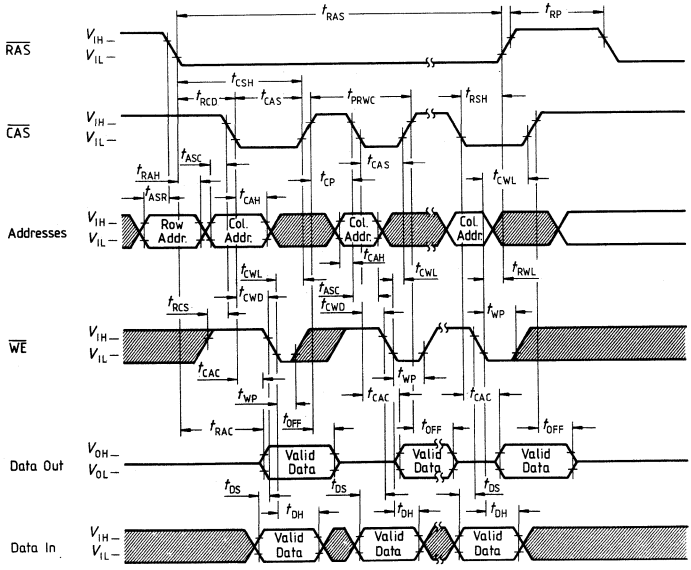
Page-Mode Read Cycle



Page-Mode Write Cycle



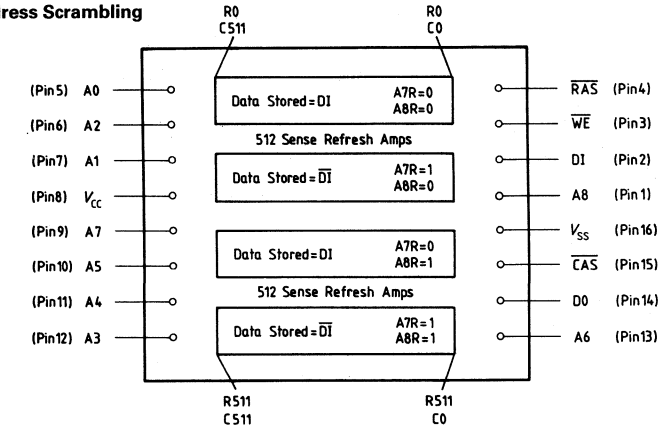
Page-Mode Read-Write Cycle



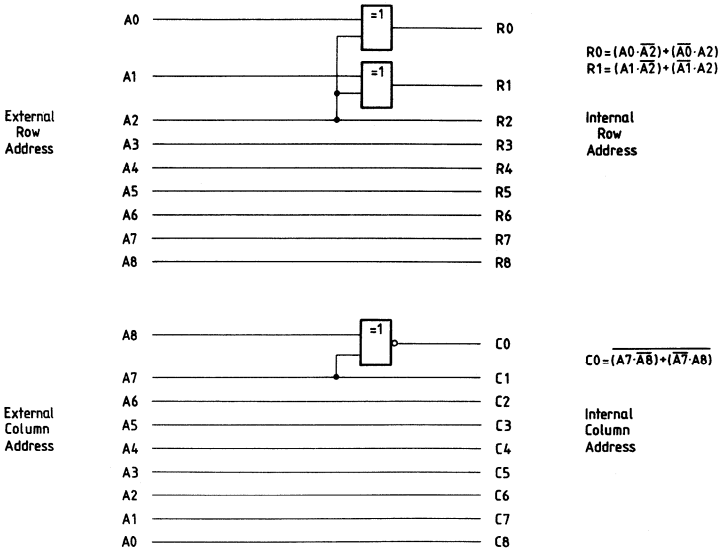
Address Decoder Scrambling (without redundancy)

The evaluation and incoming testing of RAMs normally requires a description of the internal address scrambling of the device in order to check for 'worst case' pattern.

Internal Address Scrambling



Address Decoder Scrambling



Note: The logic symbols are used solely to indicate the logic function.

Redundancy

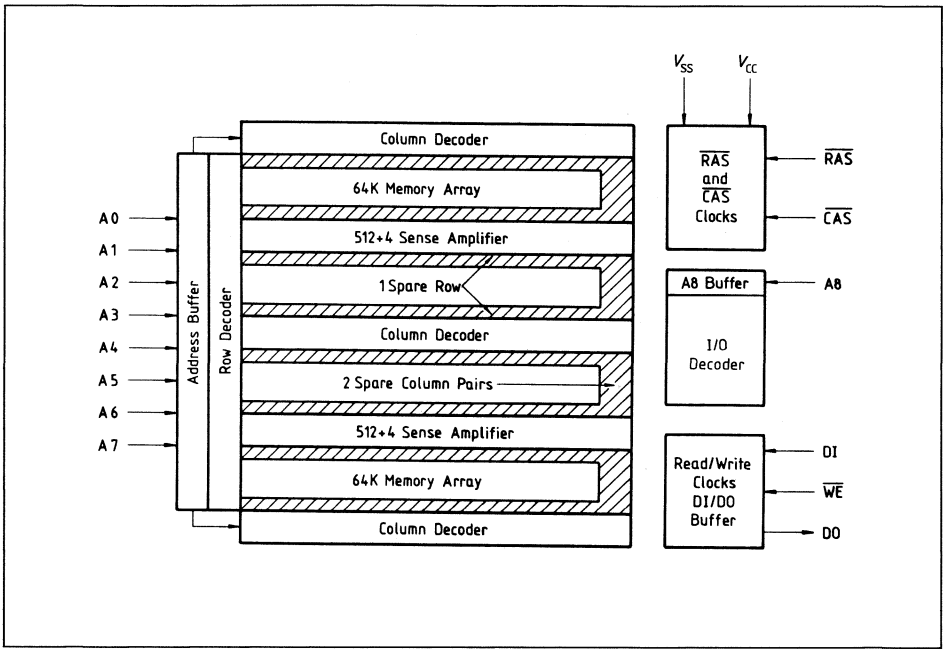
Redundancy Concept

The HYB 41256 takes advantage of the redundancy concept for increasing yield. This is done by providing the chip with a total of 8 spare rows and 4 spare column pairs. Two spare rows can be selected independently in each of four 64K cell arrays, and two spare column pairs can be selected independently in each of two 128K cell blocks. The spare lines can be selected by spare decoders which have to be programmed by laser technique during wafer probe.

Laser Technology

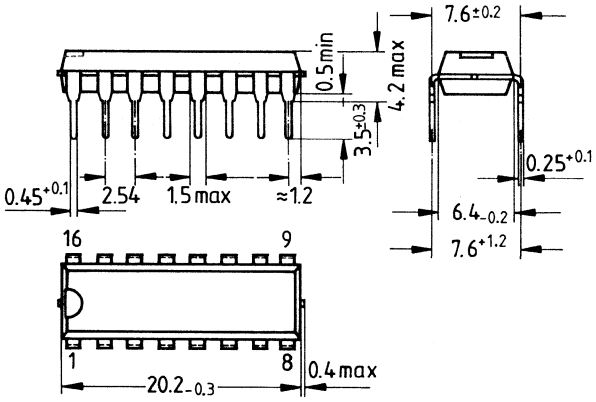
For activation of redundant circuitry a laser pulse is used to open polycide links within the spare row and spare column decoders. The laser technique is used because it is mature and has proven reliable in a number of semiconductor applications including the implementation of redundant memory circuitry. Due to the fact, that the laser beam is very fine and can easily and accurately be positioned, and that it incorporates the energy for a controlled blowup of the polycide links, the laser technique is well suited for highly complex memory circuitry. All that results in a more efficient use of chip area.

Siemens 256K DRAM Chip Topology



Package Outlines

Plastic Package, (dual-in-line-package)
P-DIP-16, 20 A 16 DIN 41870 T 9



Dimensions in mm

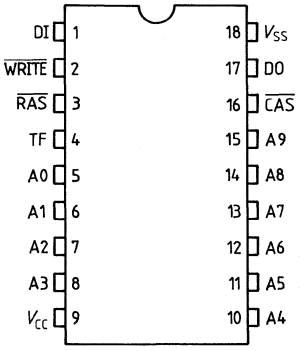
Ordering Information

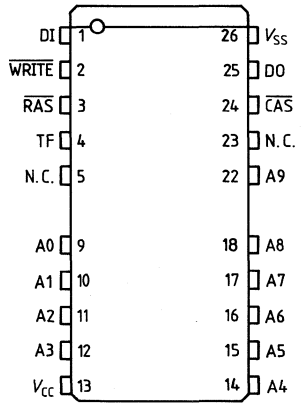
Type	Ordering Code	Description
HYB 41256-10	Q 67100-Q 380	DRAM (access time 100 ns)
HYB 41256-12	Q 67100-Q 346	DRAM (access time 120 ns)
HYB 41256-15	Q 67100-Q 347	DRAM (access time 150 ns)

HYB 511000-85/10/-12
1 048 576 Bit Dynamic RAM

- 1 048 576 words by 1-bit organization
- Fast access and cycle time
  85 ns access time
  165 ns cycle time (HYB 511000-85)
  100 ns access time
  190 ns cycle time (HYB 511000-10)
  120 ns access time
  220 ns cycle time (HYB 511000-12)
- Fast page mode cycle time
  50 ns (HYB 511000-85)
  55 ns (HYB 511000-10)
  70 ns (HYB 511000-12)
- Single +5V (±10%) supply with a built-in V_{BB} generator
- Low power dissipation
  max. 385 mW active (HYB 511000-85)
  max. 330 mW active (HYB 511000-10)
  max. 275 mW active (HYB 511000-12)
  max. 5.5 mW standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "early write" operation
- Read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, fast page mode capability and test mode capability
- All inputs and output TTL-compatible
- 512 refresh cycles/8 ms
- Plastic Packages: P-DIP-20, P-SOJ-26-20

Pin Configuration





The HYB 511000 is the new generation dynamic RAM organized as 1 048 576 words by 1-bit. The HYB 511000 utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 511000 to be packaged in a standard 18-pin or in a 26-20-pin (SOJ) plastic package.

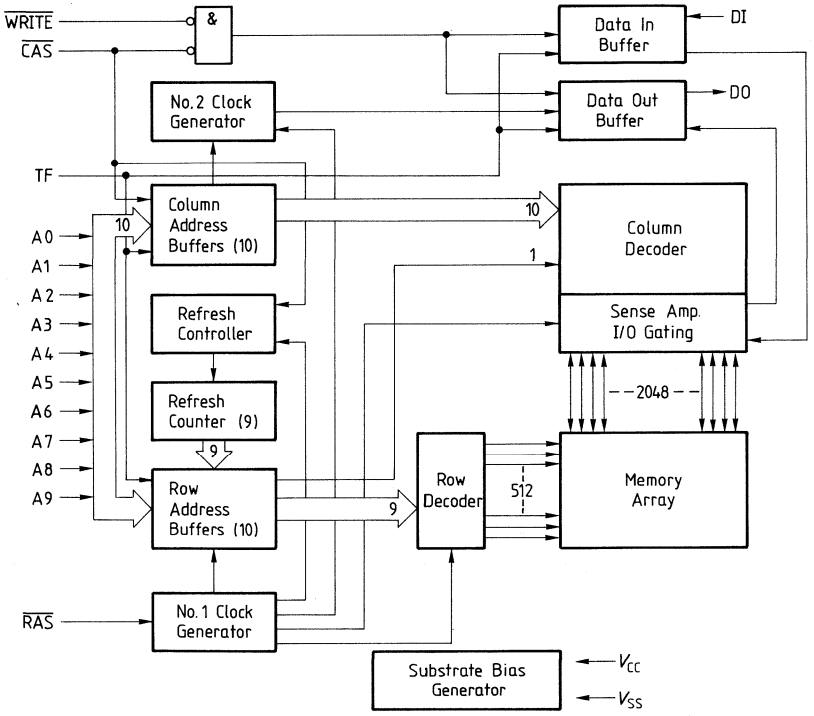
This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System-oriented features include single +5V (±10%) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

2.88

Pin Names

A0 – A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
DI	Data In
DO	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground (0 V)
TF	Test function
NC	No Connection

Block Diagram



Absolute Maximum Ratings [1]

Operating temperature range	0 to 70°C
Storage temperature range	−55 to +150°C
Soldering temperature	260°C
Soldering time	10 s
Input/Output voltage	−1 to +7 V
Test Function Input Voltage	−1 to +10.5 V
Power supply voltage	−1 to +7 V
Power dissipation	0.6 W
Data out current (short circuit)	50 mA

DC Characteristics

T_A = 0 to 70°C, V_{SS} = 0 V, V_{CC} = 5 V ± 10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	−1.0	0.8	V	–
$V_{IH\,(TF)}$	Test enable input high voltage	V_{CC}+4.5	10.5	V	–
$V_{IL\,(TF)}$	Test disable input low voltage	−1.0	V_{CC}+1.0	V	–
V_{OH}	Output high voltage (I_{OUT} = −5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current, any input except TF (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	−10	10	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	−10	10	µA	–
I_{CC1}	Average V_{CC} supply current: HYB 511000-85	–	70	mA	2) 3)
	HYB 511000-10	–	60	mA	2) 3)
	HYB 511000-12	–	50	mA	2) 3)
	($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)				
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	2	mA	–
I_{CC3}	Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles: HYB 511000-85	–	70	mA	2)
	HYB 511000-10	–	60	mA	2)
	HYB 511000-12	–	50	mA	2)
	($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.)				
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYB 511000-85	–	50	mA	2) 3)
	HYB 511000-10	–	40	mA	2) 3)
	HYB 511000-12	–	30	mA	2) 3)
	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)				

Notes see next page.

DC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC}-0.2V$)	–	1	mA	–
I_{CC6}	Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: HYB 511000-85 HYB 511000-10 HYB 511000-12 ($\overline{RAS}$, $\overline{CAS}$ cycling: $t_{RC} = t_{RC}$ min.)	– – –	70 60 50	mA mA mA	2) 2) 2)
$I_{ITF(L)}$	Input leakage current (only TF) ($0V \leq V_{IN}$ (TF) $\leq V_{CC}+0.5V$) All other pins not under test = 0V	–10	+10	µA	–
I_{TF}	Test function input current ($V_{CC} + 4.5 \leq V_{IN\,(TF)} \leq 10.5V$)	–	1	mA	–

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

3) I_{CC1}, I_{CC4} depend on output loading. Specified values are measured with the output open.

AC Characteristics [4) 5)]

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; t_T = 5 ns

Symbol	Parameter	Limit values						Unit
		HYB 511000-85		HYB 511000-10		HYB 511000-12		
		min.	max.	min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	165	–	190	–	220	–	ns
t_{RWC}	Read-write cycle time	190	–	220	–	255	–	ns
t_{PC}	Fast page mode cycle time	50	–	55	–	70	–	ns
t_{PRWC}	Fast page mode read/write cycle time	75	–	85	–	105	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6) 11)]	–	85	–	100	–	120	ns
t_{CAC}	Access time from $\overline{CAS}$ [6) 11)]	–	25	–	25	–	30	ns
t_{AA}	Access time from column address [6) 12)]	–	45	–	50	–	60	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6)]	–	45	–	50	–	65	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6)]	5	–	5	–	5	–	ns
t_{OFF}	Output buffer turn-off delay [7)]	0	30	0	30	0	35	ns
t_T	Transition time (rise and fall) [5)]	3	50	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	90	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	85	10000	100	10000	120	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	85	100000	100	100000	120	100000	ns
t_{RSH}	$\overline{RAS}$ hold time	25	–	25	–	30	–	ns
t_{CSH}	$\overline{CAS}$ hold time	85	–	100	–	120	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	25	10000	25	10000	30	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	25	60	25	75	25	90	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12]	20	40	20	50	20	60	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	10	–	10	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	15	–	ns
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns
t_{RAH}	Row address hold time	15	–	15	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns
t_{CAH}	Column address hold time	20	–	20	–	25	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns

For notes see page 411.

Symbol	Parameter	Limit values						Unit
		HYB 511000-85		HYB 511000-10		HYB 511000-12		
		min.	max.	min.	max.	min.	max.	
t_{RAL}	Column address to $\overline{RAS}$ lead time	45	–	50	–	60	–	ns
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns
t_{RCH}	Read command hold time [8]	0	–	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8]	0	–	0	–	0	–	ns
t_{WCH}	Write command hold time	20	–	20	–	25	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns
t_{WP}	Write command pulse width	20	–	20	–	25	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	20	–	25	–	30	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	20	–	25	–	30	–	ns
t_{DS}	Data setup time [9]	0	–	0	–	0	–	ns
t_{DH}	Data hold time [9]	20	–	20	–	25	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns
t_{REF}	Refresh period	–	8	–	8	–	8	ms
t_{WCS}	Write command set-up time [10]	0	–	0	–	0	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay time [10]	25	–	25	–	30	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay time [10]	85	–	100	–	120	–	ns
t_{AWD}	Column address to $\overline{WRITE}$ delay time [10]	45	–	50	–	60	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	0	–	ns
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	50	–	50	–	60	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	15	–	15	–	20	–	ns
t_{TES}	Test mode enable setup time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns
t_{TEHR}	Test mode enable hold time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns
t_{TEHC}	Test mode enable hold time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns

For notes see next page.

Capacitance

T_A = 0 to 70°C, V_{CC} = 5 V ±10%, f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
CI1	Input capacitance (A0 to A9, DI)	–	5	pF
CI2	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	pF
CO	Output capacitance (DO)	–	7	pF

Notes

[4] An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

[5] V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

[6] Measured with a load equivalent to 2 TTL loads and 100 pF.

[7] t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

[8] Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

[9] These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.

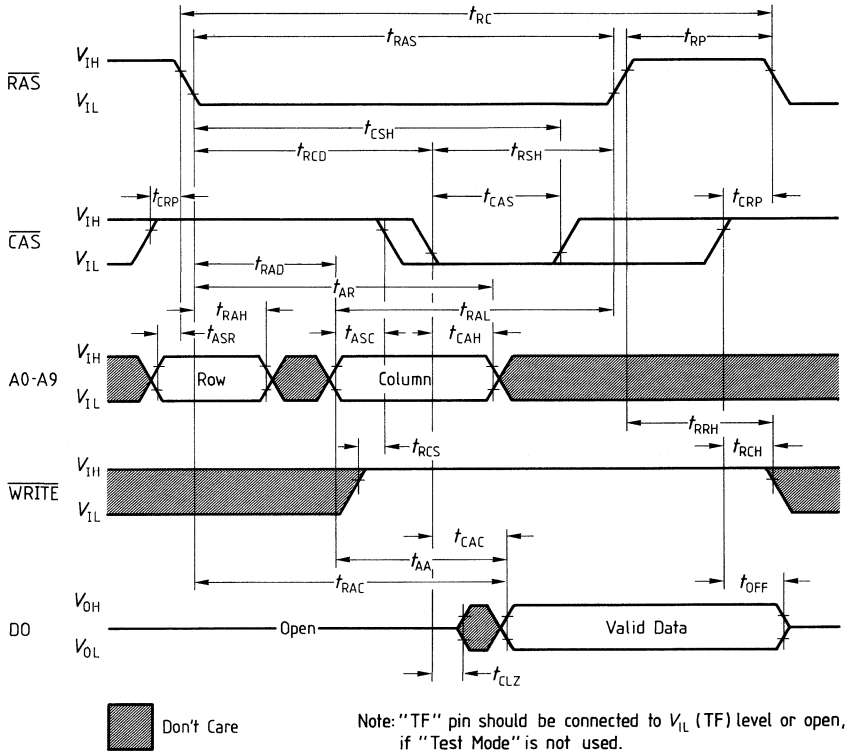
[10] t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of DO (at access time) is indeterminate.

[11] Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

[12] Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

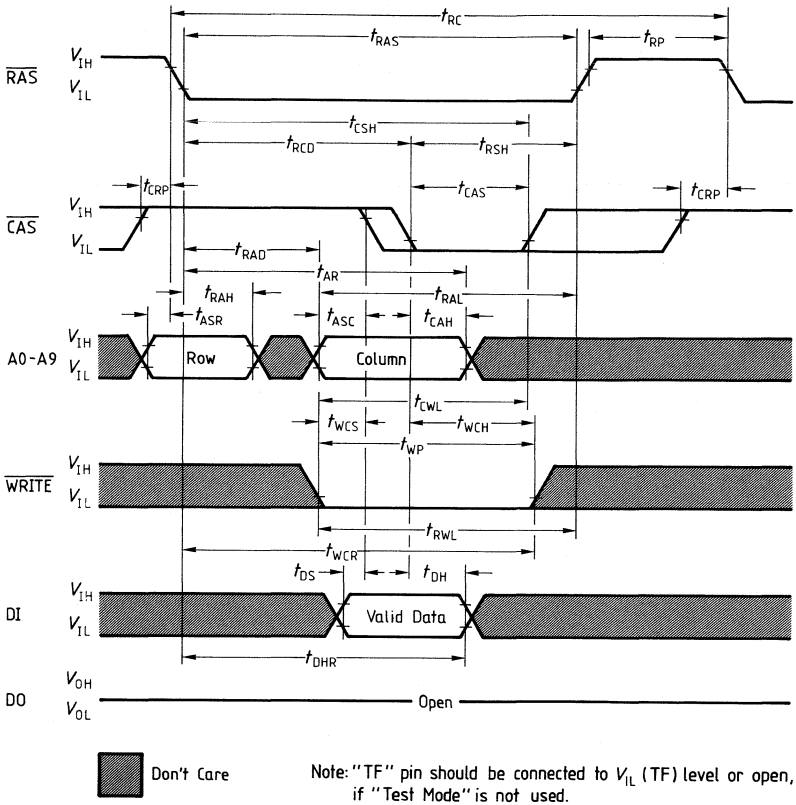
Waveforms

Read Cycle



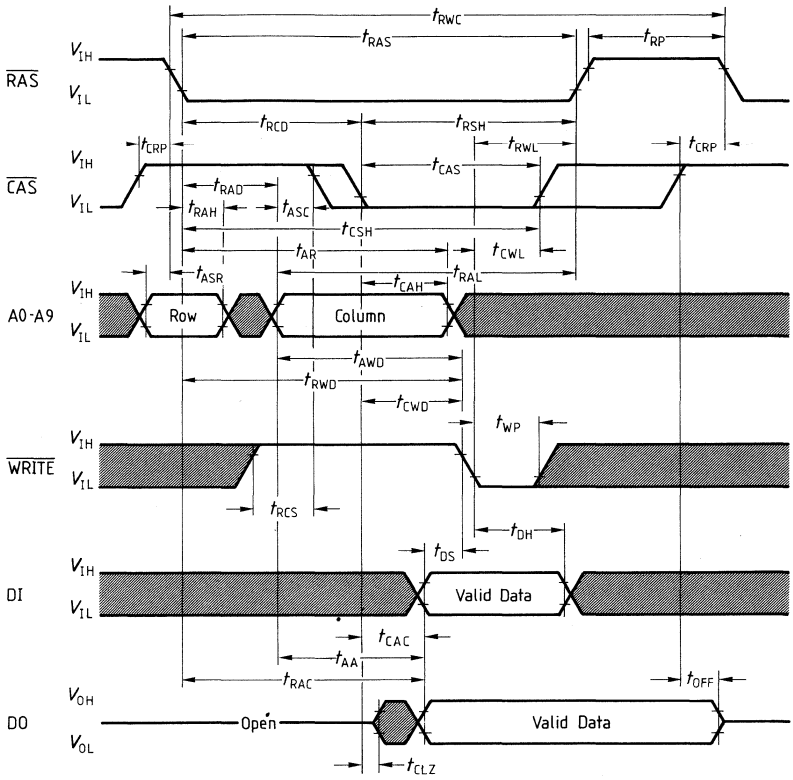
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Write Cycle (early write)

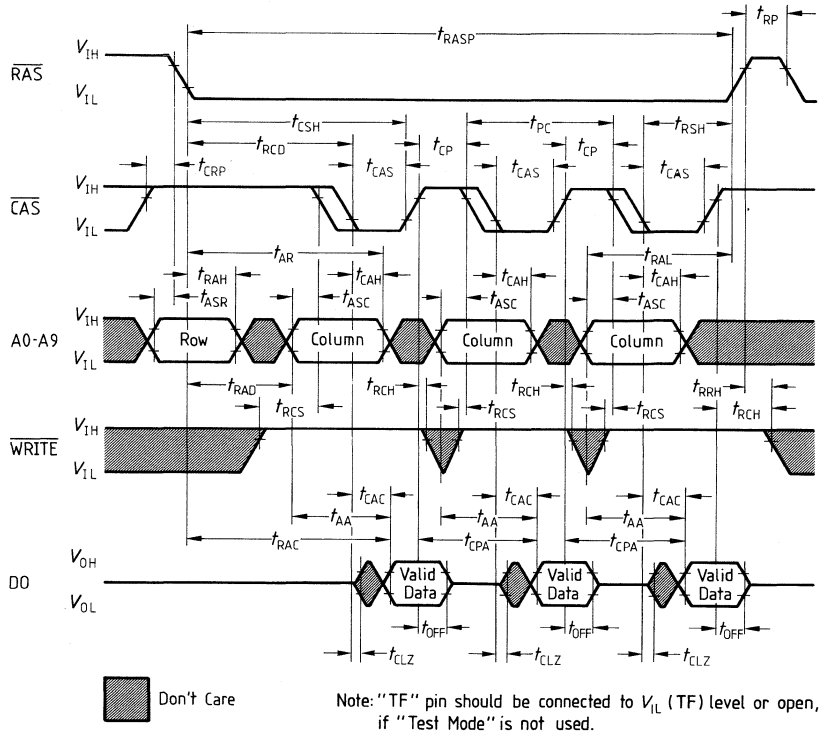


Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Read-Write Cycle

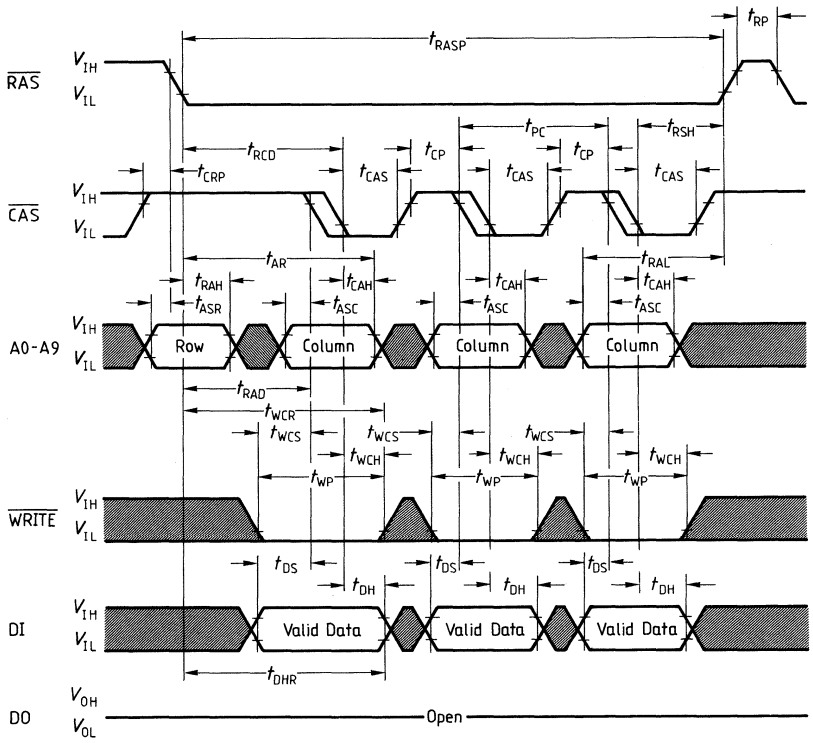


Fast Page Mode Read Cycle



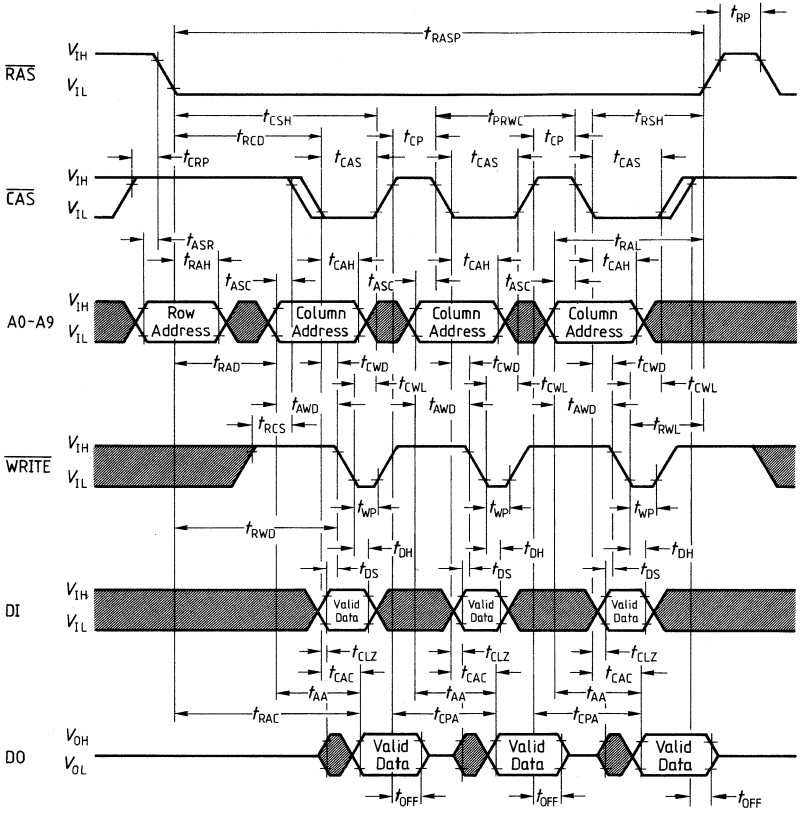
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Fast Page Mode Write Cycle (early write)



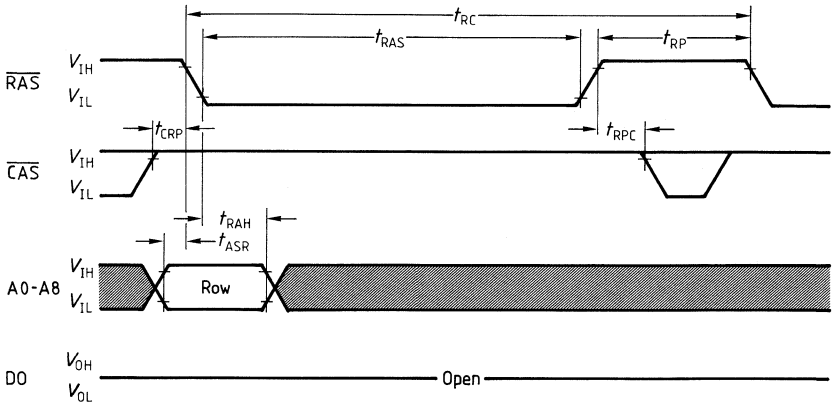
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Fast Page Mode Read-Write Cycle



Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{\text{RAS}}$-Only Refresh Cycle

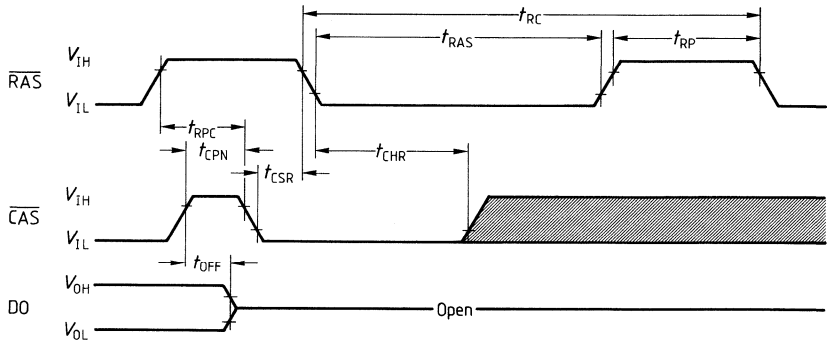


Note: $\overline{\text{WRITE}}$ = Don't Care, A9 = Don't Care

Don't Care

"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle

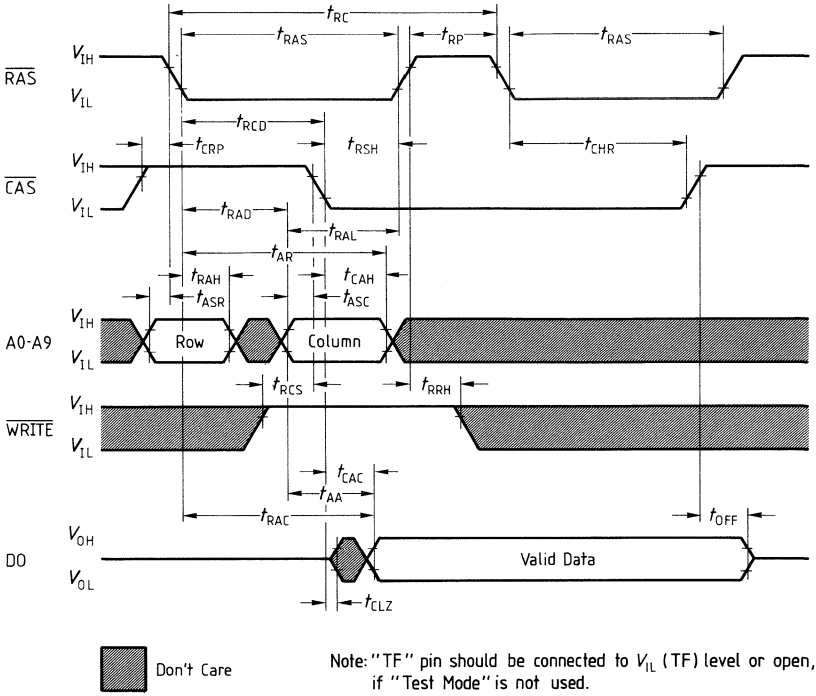


Note: $\overline{\text{WRITE}}$ = Don't Care, A0-A9 = Don't Care

Don't Care

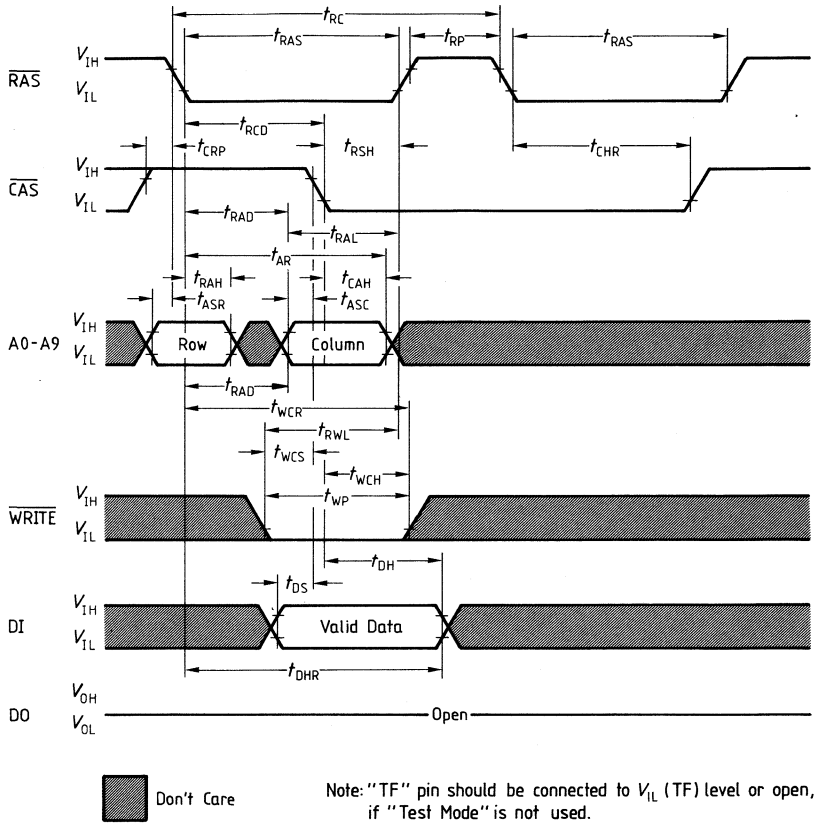
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Hidden Refresh Cycle (read)

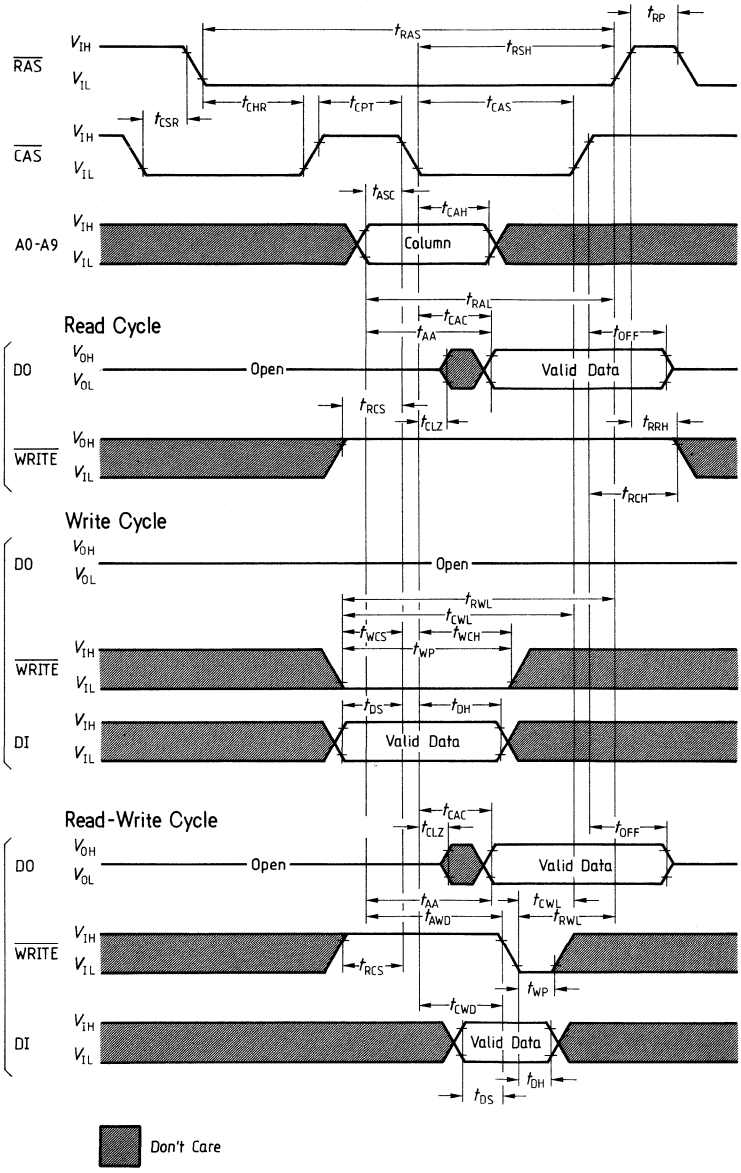


Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Hidden Refresh Cycle (write)



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle

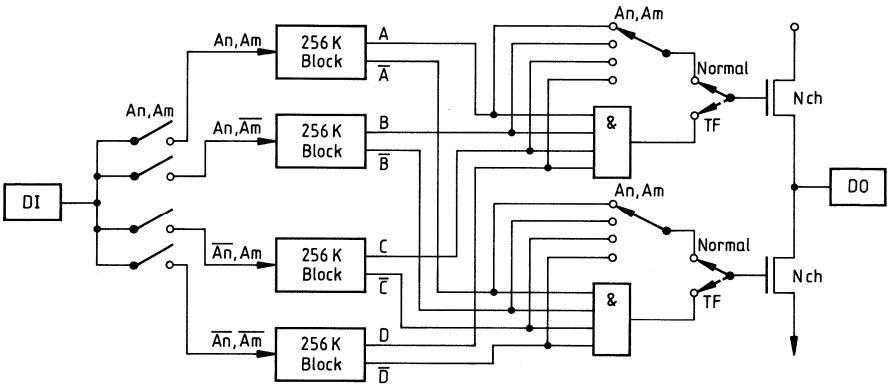


Test Mode

The HYB 511000 is the RAM organized 1 048 576 words by 1-bit, it is internally organized 262 144 words by 4-bit. In "Test Mode", data would be written into a number of sectors (4 sectors) in parallel and retrieved the same way. If upon reading, all bits are equal (all "H" or "L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. The next figure shows the block diagram including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256KDRAM by the following method.

Block Diagram in Test Mode



TF = Super voltage; Test Mode
TF = V_{IL} (TF) level or High-Z; Normal

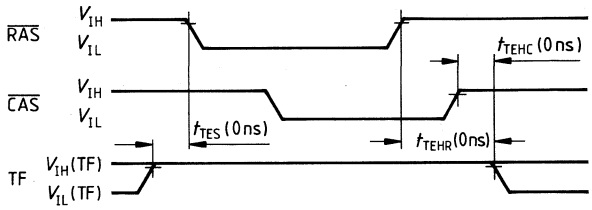
Truth Table in Test mode Function

A	B	C	D	DO
0	0	0	0	0
1	1	1	1	1
otherwise				Hi-Z

"Test Mode" function is performed on any of the timing cycles including fast page mode when "TF" pin is held on "super voltage (V_{CC} + 4.5 V (V_{CC} = 5 V ± 10%), max. voltage = 10.5 V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see next figure). The address input of A9 is ignored in the "Test Mode".

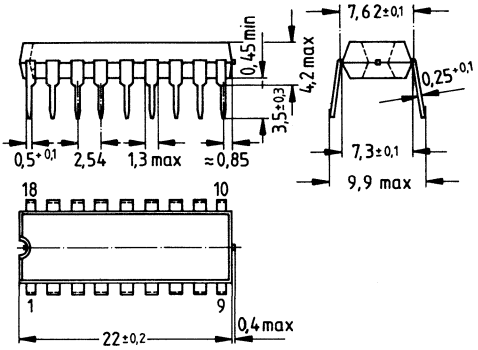
On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board.
The "Test Mode" function reduces test times (1/4; in case of using N test pattern). This "Test Mode" function is implemented from Revision "C".

Test mode cycle



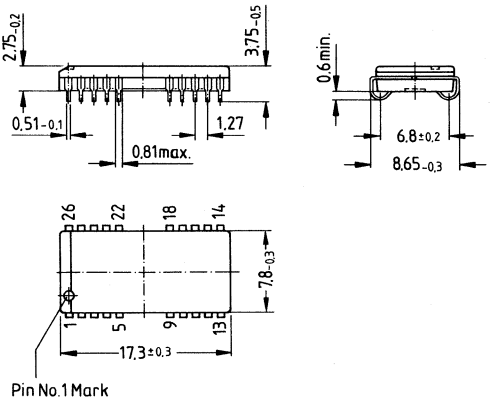
Package Outline

Plastic Package, P-DIP-18
(dual-in-line package)



Dimensions in mm

Plastic Package, P-SOJ-26-20



Dimensions in mm

Ordering Information

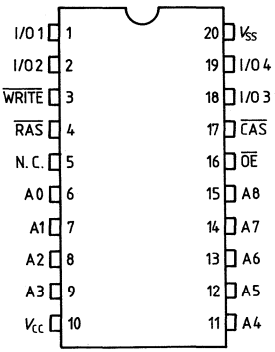
Type	Description	Ordering code
HYB 511000-85	DRAM (access time 85 ns), P-DIP-18	Q67100-Q374
HYB 511000-10	DRAM (access time 100 ns), P-DIP-18	Q67100-Q362
HYB 511000-12	DRAM (access time 120 ns), P-DIP-18	Q67100-Q363
HYB 511000J-85	DRAM (access time 85 ns) P-SOJ-26-20	Q67100-Q375
HYB 511000J-10	DRAM (access time 100 ns) P-SOJ-26-20	Q67100-Q367
HYB 51100J-12	DRAM (access time 120 ns) P-SOJ-26-20	Q67100-Q366

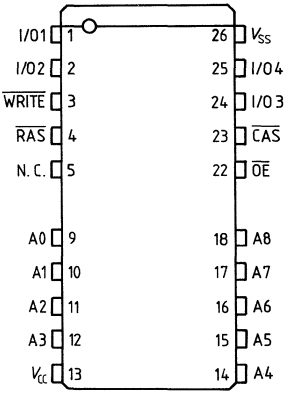
Advance Information

HYB 514256-85/-10/-12
262144x4-Bit Dynamic RAM

- 262144 words by 4-bit organization
- Fast access and cycle time
  85 ns access time
  165 ns cycle time (HYB 514256-85)
  100 ns access time
  190 ns cycle time (HYB 514256-10)
  120 ns access time
  220 ns cycle time (HYB 514256-12)
- Fast page mode cycle time
  50 ns (HYB 514256-85)
  55 ns (HYB 514256-10)
  70 ns (HYB 514256-12)
- Single +5V (±10%) supply with a built-in V_{BB} generator
- Low power dissipation
  max. 413 mW active (HYB 514256-85)
  max. 358 mW active (HYB 514256-10)
  max. 303 mW active (HYB 514256-12)
  max. 5.5 mW standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, and fast page mode capability
- All inputs and outputs TTL-compatible
- 512 refresh cycles/8 ms
- Plastic Packages: P-DIP-20
  P-SOJ-26-20

Pin Configuration





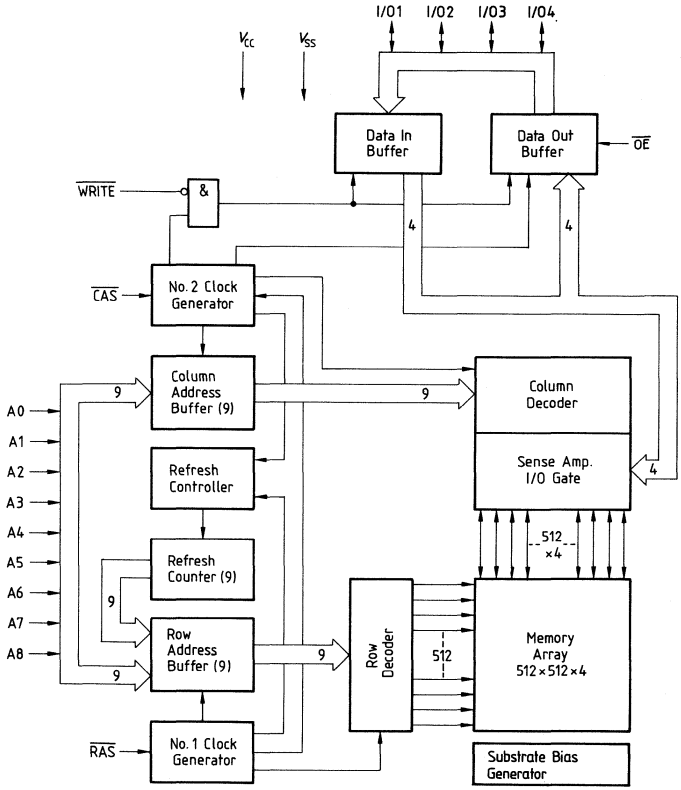
The HYB 514256 is the new generation dynamic RAM organized as 262144 words by 4-bit. The HYB 514256 utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514256 to be packaged in a standard 20-pin or in a 26-20-pin (SOJ) plastic package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. Systemoriented features include single +5V (±10%) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

3.88

Pin Names

A0 – A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/01 – I/04	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Block Diagram



Absolute Maximum Ratings [1]

Operating temperature range	0 to 70°C
Storage temperature range	−55 to +150°C
Soldering temperature	260°C
Soldering time	10 s
Input/Output voltage	−1 to +7 V
Power supply voltage	−1 to +7 V
Power dissipation	0,6 W
Data out current (short circuit)	50 mA

DC Characteristics

T_A = 0 to 70°C, V_{SS} = 0 V, V_{CC} = 5 V ± 10%

Symbol	Parameter	Limit values min.	Limit values max.	Unit	Test condition
V_{IH}	Input high voltage	2.4	6.5	V	[2]
V_{IL}	Input low voltage	−1.0	0.8	V	[2]
V_{OH}	Output high voltage (I_{OUT} = −5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current, any input (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	−10	10	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC})	−10	10	µA	–
I_{CC1}	Average V_{CC} supply current: HYB 514256-85	–	75	mA	[3] [4]
	HYB 514256-10	–	65	mA	[3] [4]
	HYB 514256-12	–	55	mA	[3] [4]
	($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)				
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	2	mA	–
I_{CC3}	Average V_{CC} supply current, $\overline{RAS}$ only mode: HYB 514256-85	–	75	mA	[3]
	HYB 514256-10	–	65	mA	[3]
	HYB 514256-12	–	55	mA	[3]
	($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.)				
I_{CC4}	Average V_{CC} supply current, fast page mode: HYB 514256-85	–	55	mA	[3] [4]
	HYB 514256-10	–	45	mA	[3] [4]
	HYB 514256-12	–	35	mA	[3] [4]
	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$,address cycling: t_{PC} = t_{PC} min.)				
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}−0.2V)	–	1	mA	–
I_{CC6}	Average V_{CC} supply current, $\overline{CAS}$-before-$\overline{RAS}$ mode: HYB 514256-85	–	75	mA	[3]
	HYB 514256-10	–	65	mA	[3]
	HYB 514256-12	–	55	mA	[3]
	($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)				

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] All voltages are reference to V_{SS}.

[3] I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

[4] I_{CC1}, I_{CC4} depend on output loading. Specified values are measured with the output open.

AC Characteristics [5) 6)]

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; t_T = 5 ns

Symbol	Parameter	Limit values						Unit
		HYB 514256-85		HYB 514256-10		HYB 514256-12		
		min.	max.	min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	165	–	190	–	220	–	ns
t_{RMW}	Read-modify-write cycle time	225	–	255	–	295	–	ns
t_{PC}	Fast page mode cycle time	50	–	55	–	70	–	ns
t_{PRMW}	Fast page mode read-modify-write cycle time	110	–	115	–	140	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [7) 12)]	–	85	–	100	–	120	ns
t_{CAC}	Access time from $\overline{CAS}$ [7) 12)]	–	30	–	30	–	35	ns
t_{AA}	Access time from column address [7) 13)]	–	45	–	50	–	60	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [7) 13)]	–	45	–	50	–	65	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [5)]	5	–	5	–	5	–	ns
t_{OFF}	Output buffer turn-off delay [8)]	0	30	0	30	0	35	ns
t_T	Transition time (rise and fall) [6)]	3	50	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	90	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	85	10000	100	10000	120	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	85	100000	100	100000	120	100000	ns
t_{RSH}	$\overline{RAS}$ hold time	30	–	30	–	35	–	ns
t_{CSH}	$\overline{CAS}$ hold time	85	–	100	–	120	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	30	10000	30	10000	35	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	25	55	25	70	25	85	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [13]	20	40	20	50	20	60	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	10	–	10	–	10	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	15	–	15	–	20	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	15	–	ns
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns
t_{RAH}	Row address hold time	15	–	15	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns
t_{CAH}	Column address hold time	20	–	20	–	25	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	45	–	50	–	60	–	ns
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns
t_{RCH}	Read command hold time [9)]	0	–	0	–	0	–	ns

For notes see page 432.

Symbol	Parameter	Limit values						Unit
		HYB 514256-85		HYB 514256-10		HYB 514256-12		
		min.	max.	min.	max.	min.	max.	
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [9]	0	–	0	–	0	–	ns
t_{WCH}	Write command hold time	20	–	20	–	25	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns
t_{WP}	Write command pulse width	20	–	20	–	25	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	20	–	25	–	30	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	20	–	25	–	30	–	ns
t_{DS}	Data setup time [10]	0	–	0	–	0	–	ns
t_{DH}	Data hold time [10]	20	–	20	–	25	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns
t_{REF}	Refresh period	–	8	–	8	–	8	ms
t_{WCS}	Write command set-up time [11]	0	–	0	–	0	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay time [11]	65	–	65	–	75	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay time [11]	120	–	135	–	160	–	ns
t_{AWD}	Column address to $\overline{WRITE}$ delay time [11]	80	–	85	–	100	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	0	–	ns
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	50	–	50	–	60	–	ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	20	–	20	–	20	–	ns
t_{OEA}	$\overline{OE}$ access time	–	25	–	25	–	30	ns
t_{OED}	$\overline{OE}$ to data delay	25	–	25	–	30	–	ns
t_{OEZ}	Output buffer turn off delay time from $\overline{OE}$	0	25	0	25	0	30	ns
t_{OEH}	$\overline{OE}$ command hold time	25	–	25	–	30	–	ns

For notes see next page.

Capacitance

T_A = 0 to 70°C, V_{CC} = 5V ±10%, f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
CI1	Input capacitance (A0 to A8)	–	5	pF
CI2	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
CO	Output capacitance (I/01 ... I/04)	–	7	pF

Notes

[5] An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

[6] V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

[7] Measured with a load equivalent to 2 TTL loads and 100 pF.

[8] t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

[9] Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

[10] These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-modify-write cycles.

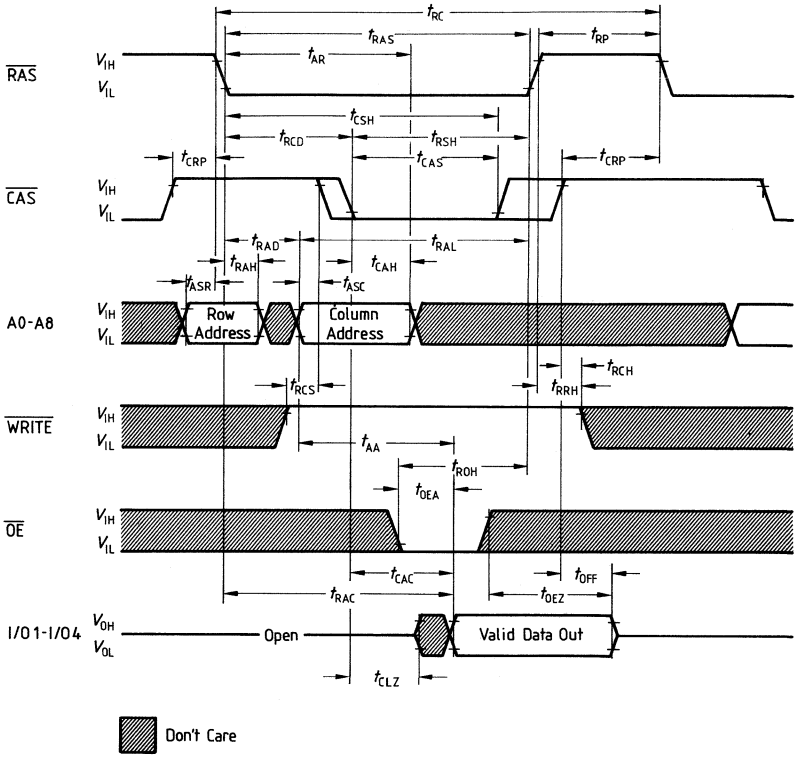
[11] t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out (at access time) is indeterminate.

[12] Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

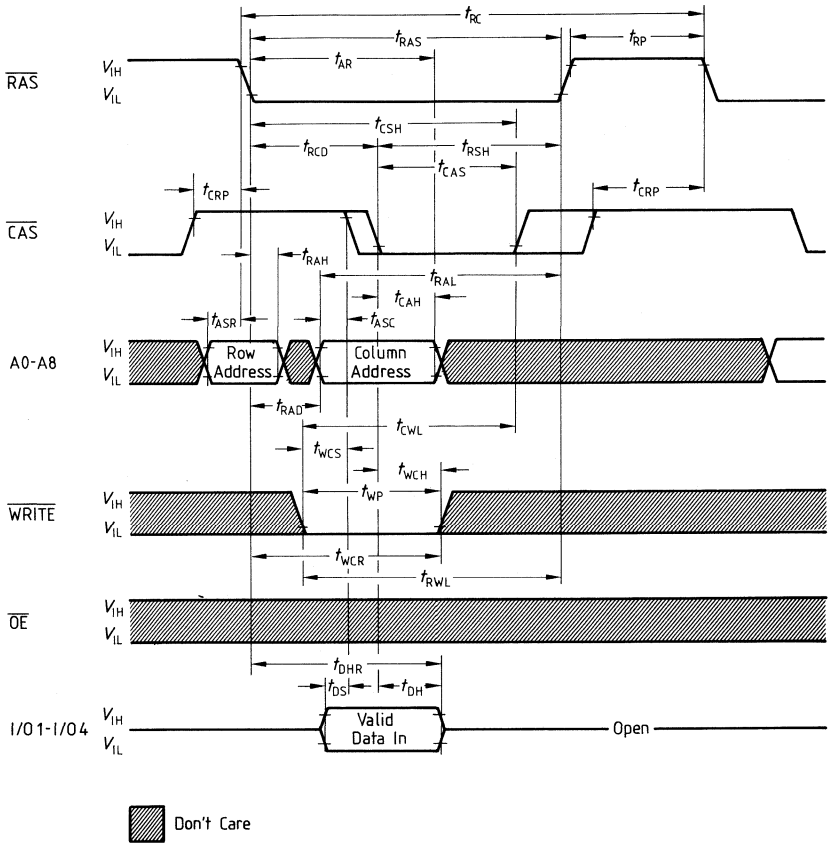
[13] Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

Waveforms

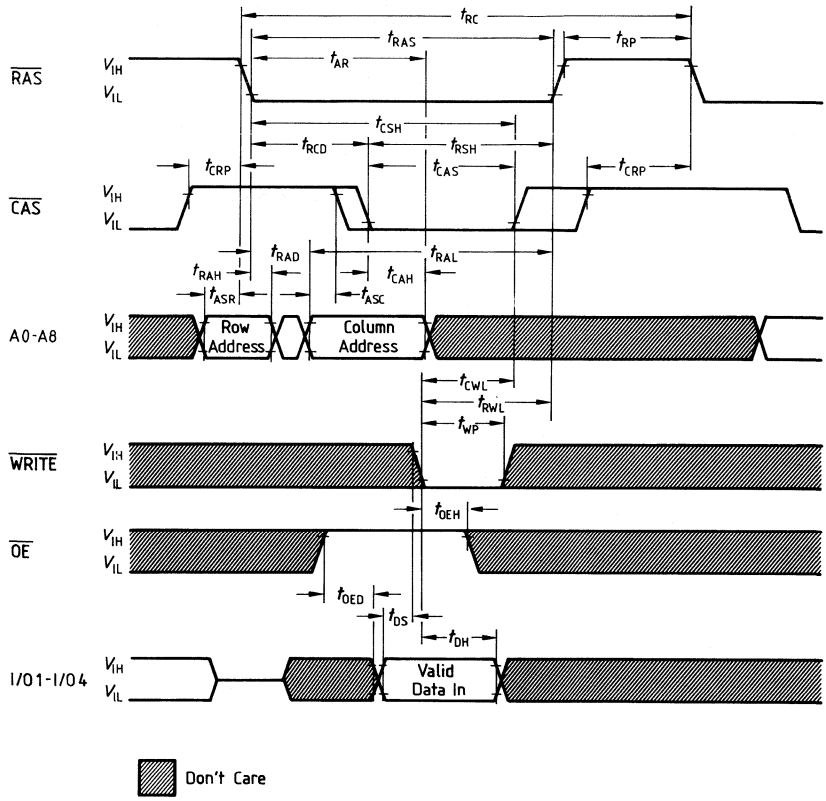
Read Cycle



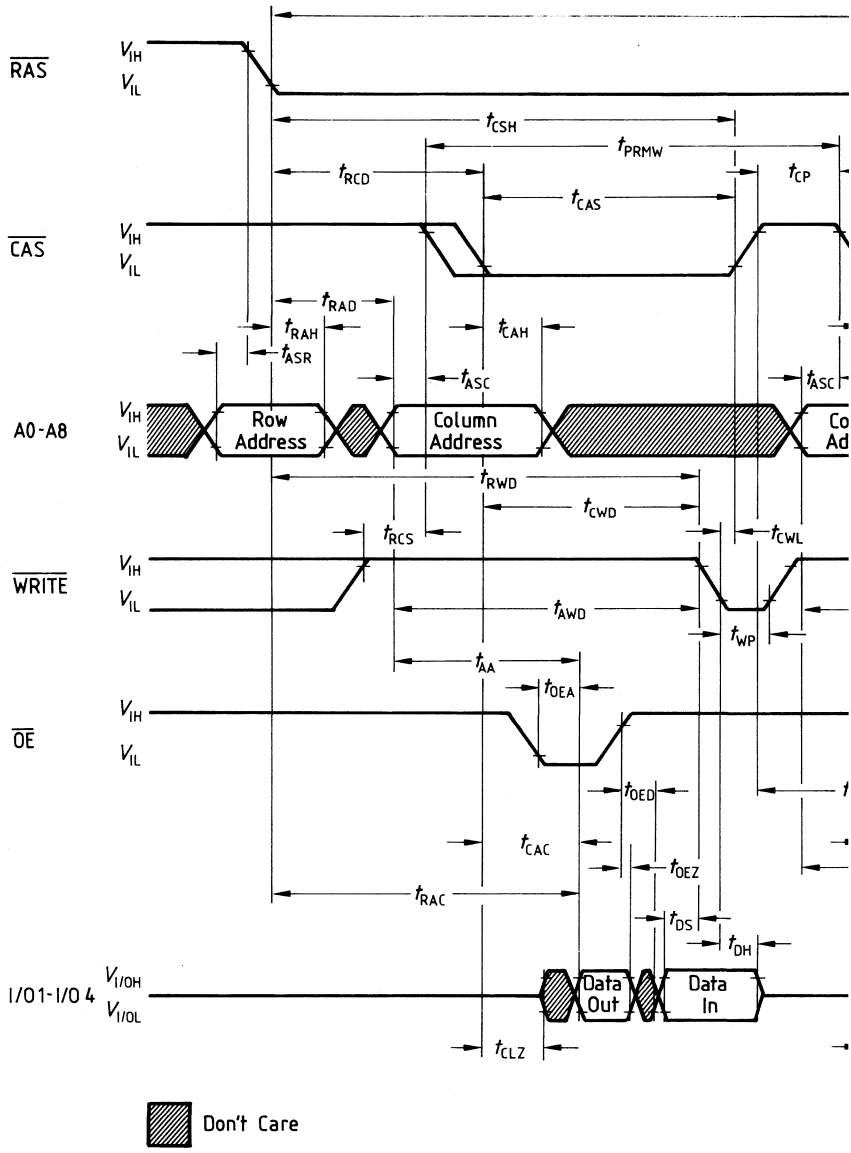
Write Cycle (Early Write)

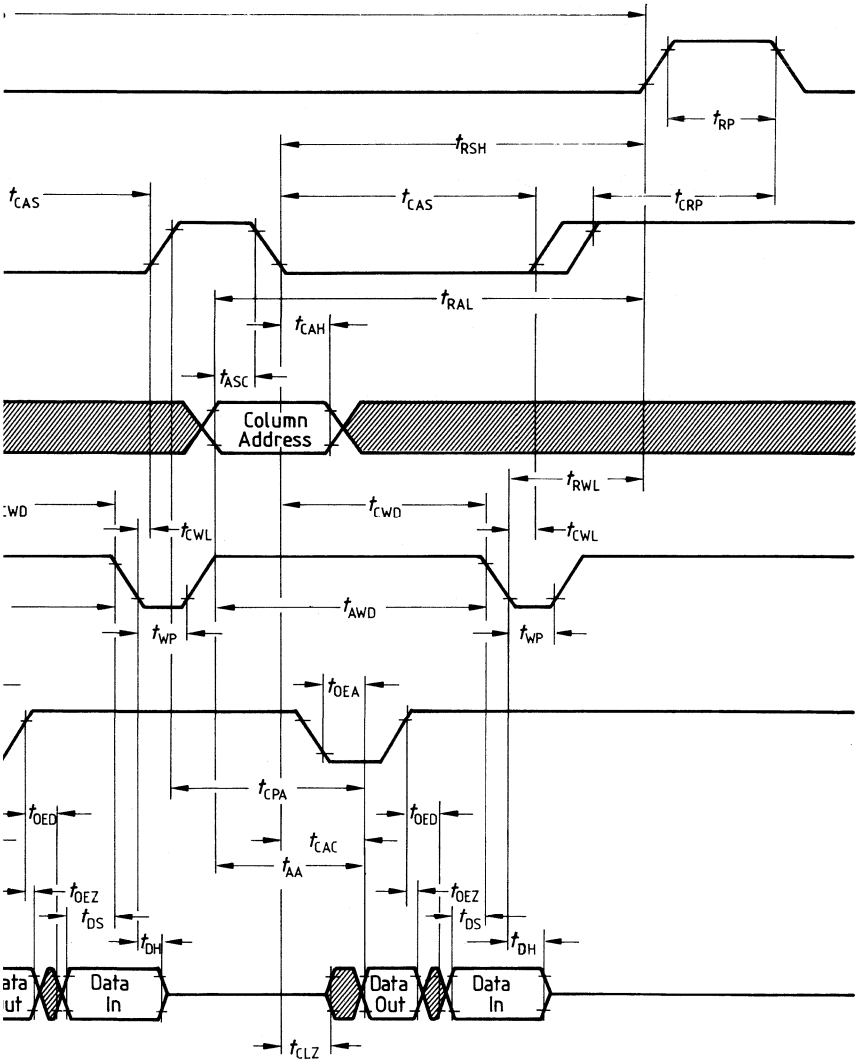


Write Cycle ($\overline{OE}$ Controlled Write)

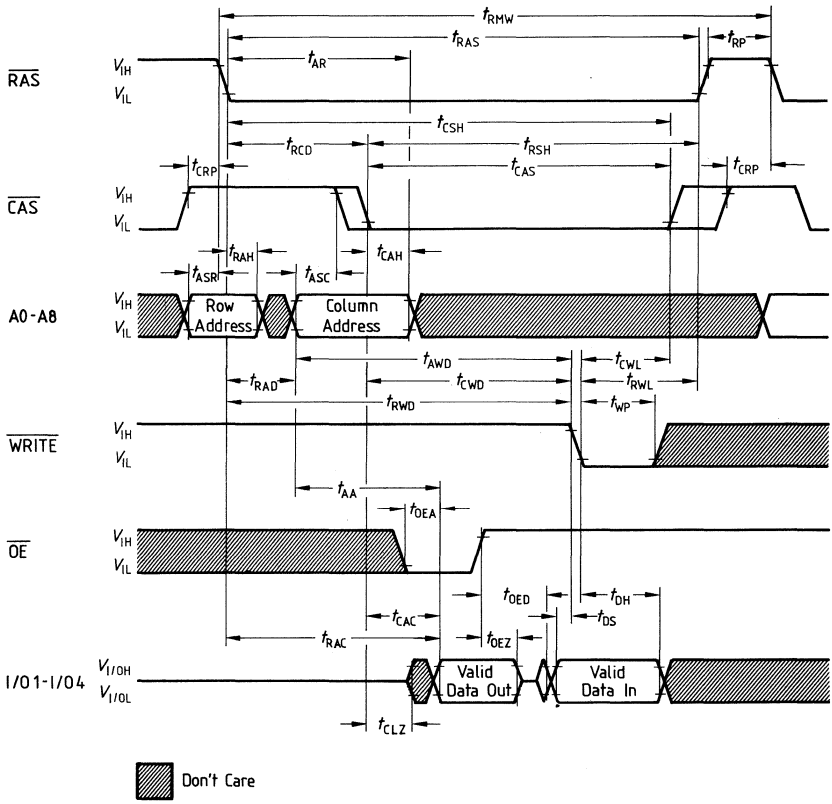


Fast Page Mode Read-Modify-Write Cycle

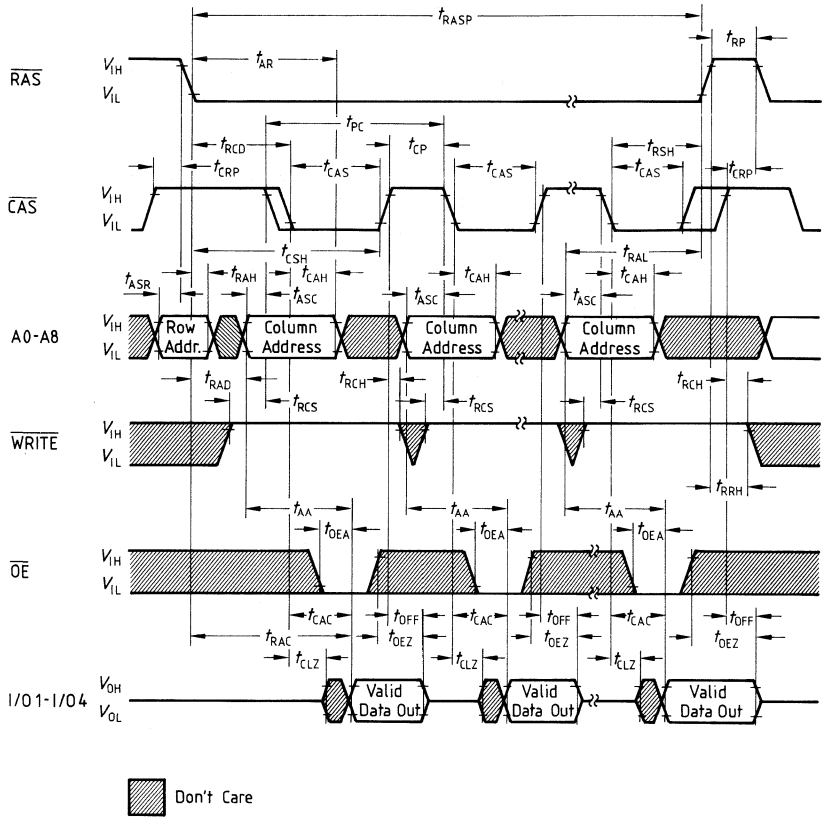



t_{RP}
t_{RSH}
t_{CAS}
t_{CAS}
t_{CRP}
t_{RAL}
t_{CAH}
t_{ASC}
Column Address
t_{RWL}
t_{CWD}
t_{CWL}
t_{CWL}
t_{AWD}
t_{WP}
t_{WP}
t_{OEA}
t_{CPA}
t_{OED}
t_{OED}
t_{CAC}
t_{AA}
t_{OEZ}
t_{DS}
t_{DH}
t_{OEZ}
t_{DS}
t_{DH}
Data In
Data Out
Data In
t_{CLZ}

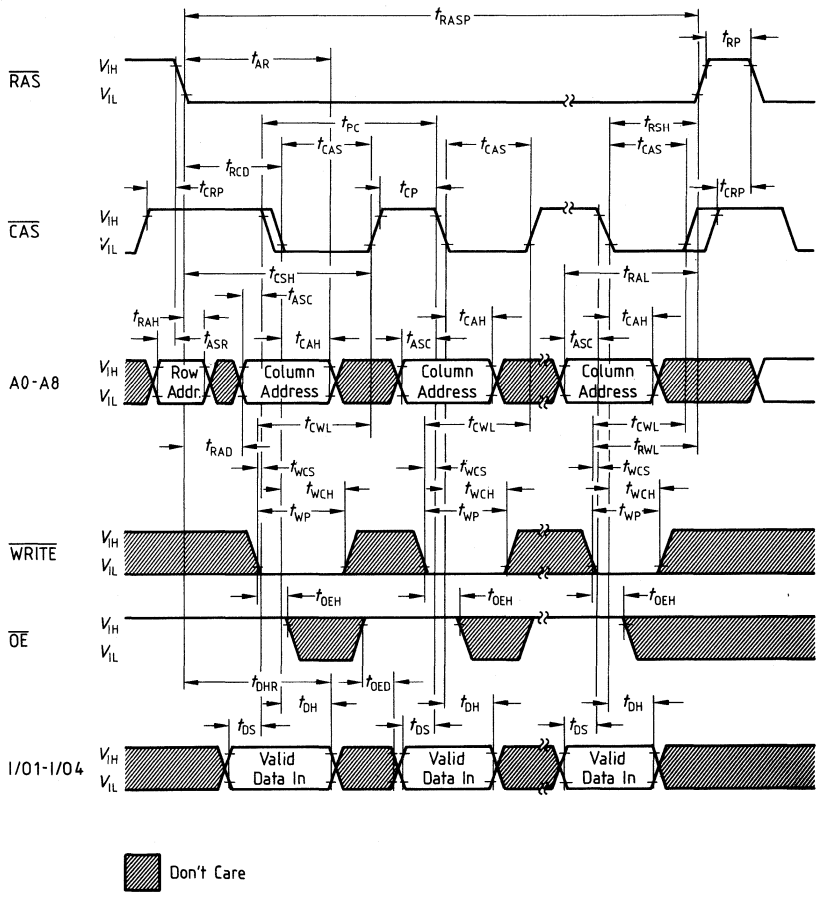
Read-Write (Read-Modify-Write) Cycle



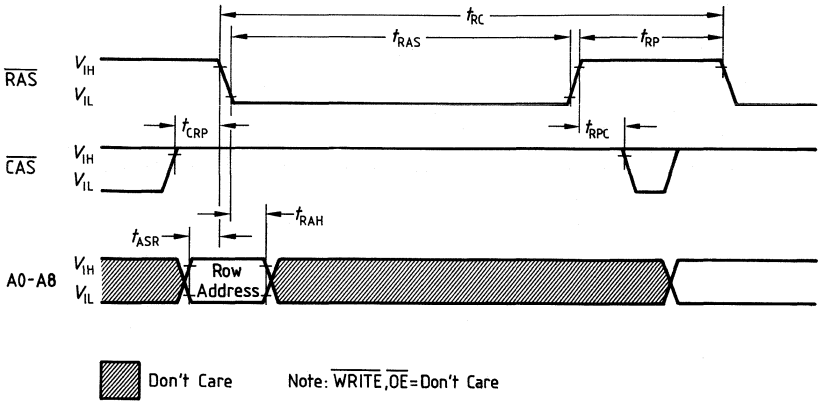
Fast Page Mode Read Cycle



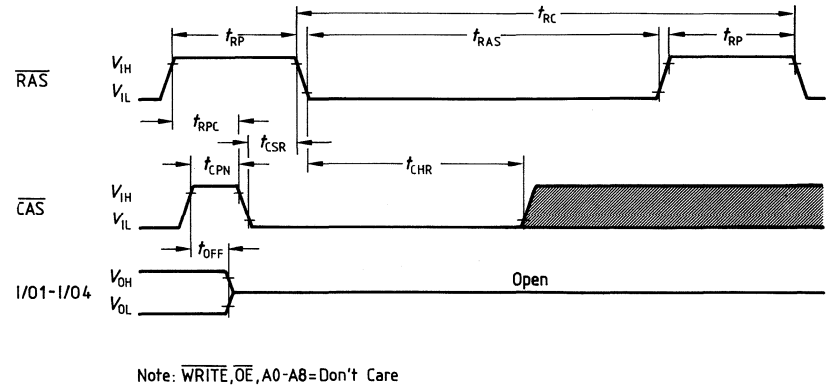
Fast Page Mode Write Cycle



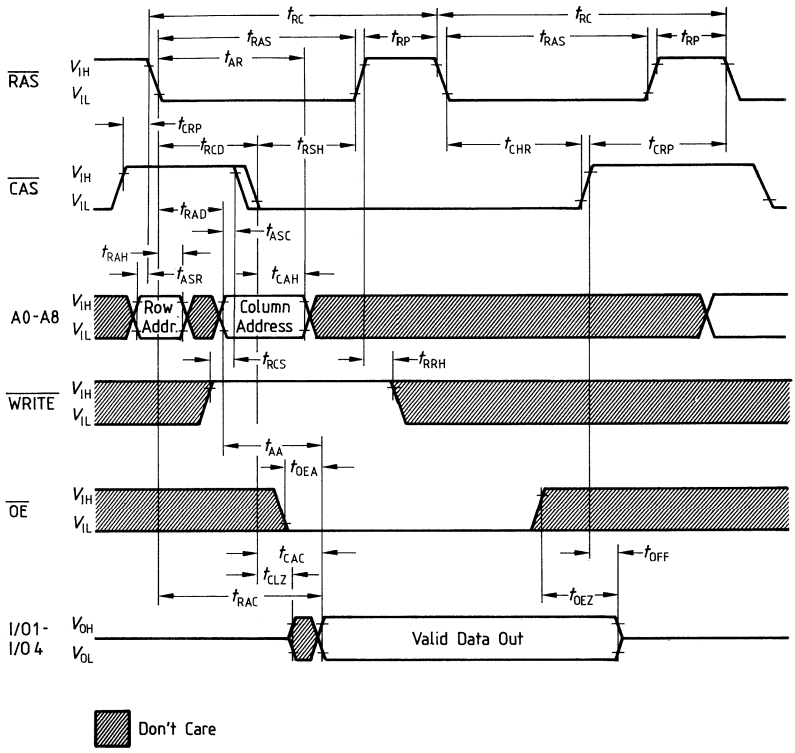
$\overline{\text{RAS}}$-Only Refresh Cycle



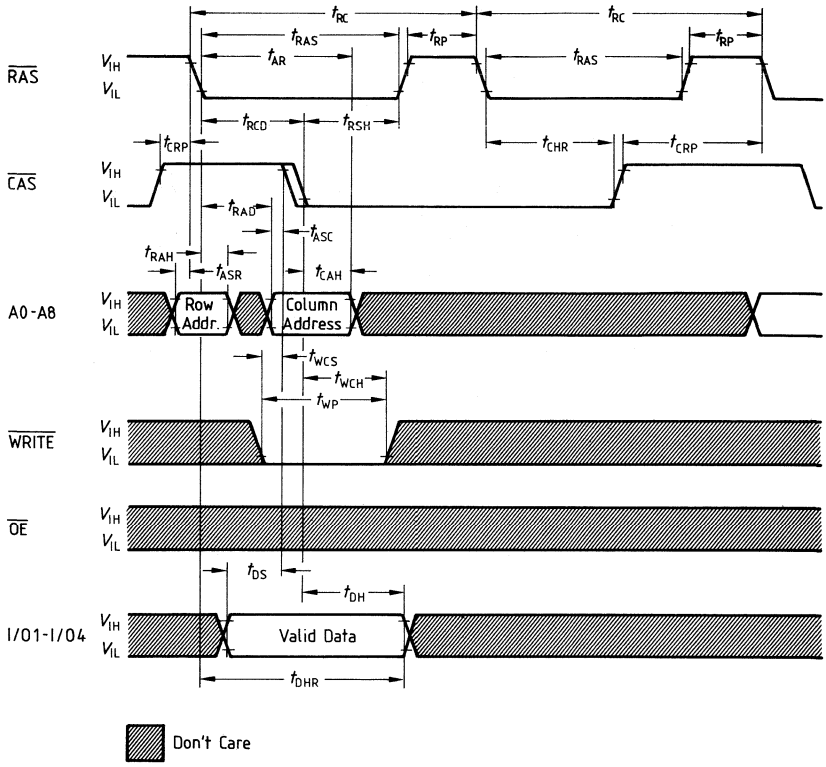
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



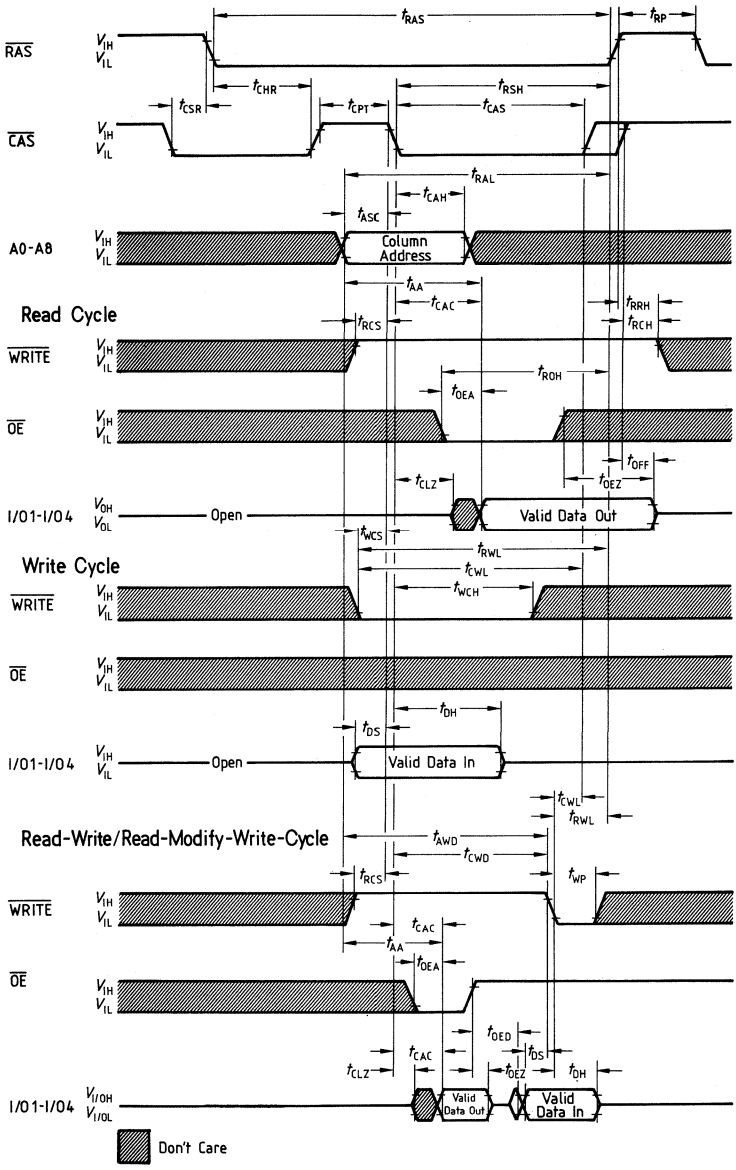
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (write)

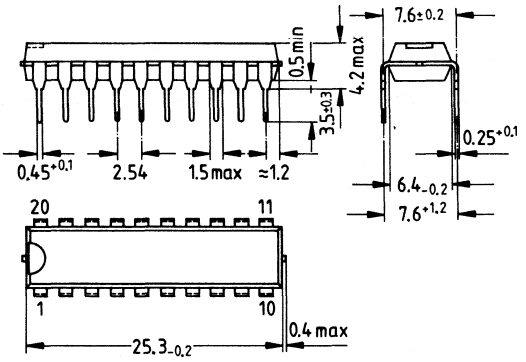


CAS-Before-RAS Refresh Counter Test Cycle



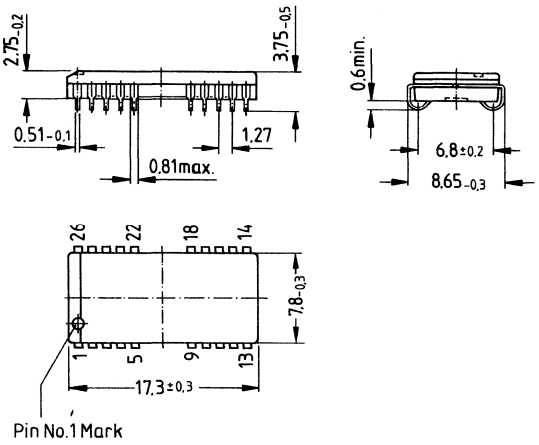
Package Outline

Plastic Package, P-DIP-20
(dual-in-line-package)
20A20DIN41870 Tg



Dimensions in mm

Plastic Package, P-SOJ-26-20



Dimensions in mm

Ordering Information

Type	Ordering Code	Description
HYB 514256-85	Q67100-Q378	DRAM (access time 85 ns), DIP 18
HYB 514256-10	Q67100-Q372	DRAM (access time 100 ns), DIP 18
HYB 514256-12	Q67100-Q373	DRAM (access time 120 ns), DIP 18
HYB 514256J-85	Q67100-Q379	DRAM (access time 85 ns), SOJ-26-20
HYB 514256J-10	Q67100-Q371	DRAM (access time 100 ns), SOJ-26-20
HYB 514256J-12	Q67100-Q370	DRAM (access time 120 ns), SOJ-26-20

Dual Port RAM
SAE 81C80

Preliminary Data **ACMOS IC**

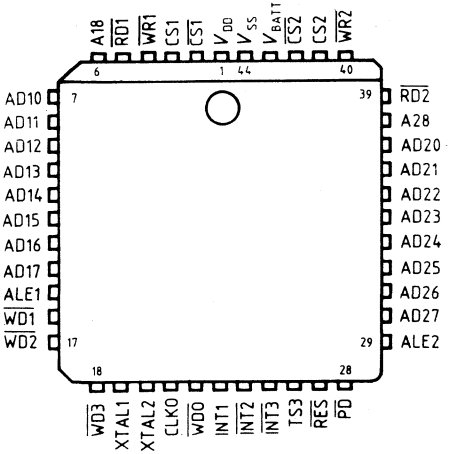
Type	Ordering Code	Package
SAE 81C80	Q67100-H8390	PLCC 44

The SAE 81C80 dual port RAM (DPR) is a CMOS memory IC with two processor interfaces and a capacity of 504 bytes. It enables the exchange of data between two processors without handshake signals and without wait states. Eight scheduling registers support the management of data areas or external resources.

Features

- ACMOS technology
- All functions fully static
- SAB 8048/8051/80515 and 8096 compatible
- Memory capacity 504 bytes and 8 scheduling registers
- On-chip oscillator with separate clock output
- 3 loadable counters for processor monitoring or as longterm counters
- Hardware watchdog
- Both processors can operate fully asynchronously
- Data retention down to 1 V
- TTL-, NMOS- and CMOS-compatible
- Extended temperature range from −40 °C to +85 °C
- Package: PLCC 44

Pin Configuration



Pin Description

Pin	Symbol	Function
7	AD10	Data and address bus port 1
8	AD11	
9	AD12	
10	AD13	
11	AD14	
12	AD15	
13	AD16	
14	AD17	
6	A18	Address 8 port 1
37	AD20	Data and address bus port 2
36	AD21	
35	AD22	
34	AD23	
33	AD24	
32	AD25	
31	AD26	
30	AD27	
38	A28	Address 8 port 2

Pin Description

Pin	Symbol	Function
15 29	ALE1 ALE2	Address latch enable port 1 Address latch enable port 2 These signals serve to separate data from addresses on the bus. The address is stored on the falling edge of the signal.
5 39	$\overline{RD1}$ $\overline{RD2}$	Read signal port 1 (active low) Read signal port 2 (active low)
4 40	$\overline{WR1}$ $\overline{WR2}$	Write signal port 1 (active low) Write signal port 2 (active low)
3	CS1	Chip select port 1
2	$\overline{CS1}$	Chip select port 1 (active low)
41 42	CS2 $\overline{CS2}$	Chip select port 2 Chip select port 2 (active low) The chip select inputs select a port when both inputs have active level.
27	$\overline{RES}$	Reset input Resets the IC to a defined start state. Simultaneously, the outputs $\overline{WDO}$, $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$ are switched to low for the duration of the reset pulse. The oscillator is not affected.
28	$\overline{PD}$	Power down. Disables all inputs and the oscillator
44 1 43	V_{SS} V_{DD} V_{BATT}	Negative supply voltage Positive supply voltage Connection for battery (negative pole, positive pole of the battery must be connected to V_{DD})
19 20 21	XTAL1 XTAL2 CLKO	Quartz connection (must be open for external clock supply) Quartz connection or external clock supply Clock output
22	$\overline{WDO}$	Oscillator watchdog (open drain output) High indicates that oscillator is in operation
16 17 18	$\overline{WD1}$ $\overline{WD2}$ $\overline{WD3}$	(Open drain output) (Open drain output) (Open drain output) } outputs of the 3 timers
26	TS3	Hardware signal to start timer B
23 24	$\overline{INT1}$ $\overline{INT2}$	(Open drain output, active low) (Open drain output, active low)
25	$\overline{INT3}$	(Open drain output, active low) Outputs that can be controlled via the port, for example, to generate an interrupt at one of the processors.

Functional Description

Dual Port RAM

The dual port RAM has a capacity of 504 bytes, which can be accessed by both processors. The memory locations are selected via a multiplexed address and data bus and two chip select inputs. The $\overline{RD}$ and $\overline{WR}$ inputs define the direction of data transfer. During simultaneous access to the same memory location, no undefined states occur, especially not in such cases, when both processors write to the same memory location. Depending on the internal status of the access control, and of the real physical sequence, the value of one of the ports will be stored. Even during simultaneous reading of and writing to the same memory location, there will be no mixing of data, i.e. either the old data or the new data will be read.

Interrupt Outputs

The dual port RAM has three outputs that can be directly set and reset by writing to an address **(table 1)**. The interrupt outputs are located in the same address range as the scheduling registers. However, only bit 2 and bit 3 are relevant for the interrupt outputs.

In order not to affect the scheduling registers, at least one of the bits 0 or 1 should not be "0". The function of the outputs is shown in the diagram to follow.

RES	Bit 3	Bit 2	Output
1	0	0	no change
1	0	1	1
1	1	0	0
1	1	1	undefined
0	—	—	1

Reset

The reset is necessary to set the DPR control circuits into a defined start state. During a reset, the timer mode registers are loaded with the value $0000XXX0_8$ (for timers 1 and 2), or with $00000XX0_8$ (for timer 3). The $\overline{INT}$ outputs are set to "1".

While the reset input is low, outputs $\overline{WD1}$, $\overline{WD2}$ and $\overline{WD3}$ are set low. After the reset pulse these outputs are high.

A reset is also necessary when the DPR is activated again from the power down mode. The contents of the RAM and the oscillator are not affected by the reset.

Power Down

When the power down pin is activated, all inputs and the oscillator are disabled, so that any levels are allowed at the remaining inputs.

Battery Connection

An external battery can be connected to pin V_{BATT}. The negative pole connects to pin V_{BATT}, the positive pole to V_{DD}. During failure of the normal supply voltage at V_{DD} the RAM will be automatically supplied from the battery so that the RAM contents are saved. All other information is lost. If no battery is used, V_{BATT} must be connected to V_{DD}.

Scheduling Register

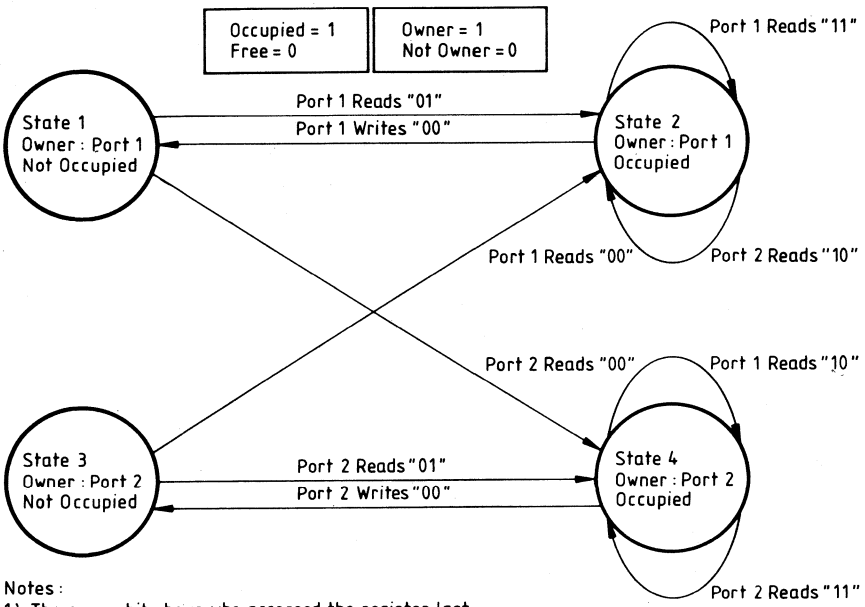
Special circuits within the dual port RAM prevent a mixing of data from the two ports. With continuous data over several bytes, it is possible that old and new data is read at one port if the other port writes to the same memory region at the same time. In order to avoid this conflict, the dual port RAM has 8 scheduling registers. Any of these registers can be used by a processor to indicate that it is accessing a data region assigned to this register. In order to make the operation with these registers as simple as possible, they have special features:

They are 2 bit registers (bit 0, bit 1 of the byte). Bit 0 indicates who "owns" the register and bit 1 indicates that it is occupied. The appropriate bits are already set during a reading of these registers, and the processor receives the correct values **(fig. 1).** Reset is achieved by writing the value "XXXXXX11$_B$". If a read access is attempted from both ports simultaneously, port 1 is given priority and port 2 receives the corresponding message.

The assignment of the scheduling registers to a location in the RAM is done by software. This means, the user is completely flexible in the assignment of the registers. It is, for example, also possible to use these registers as access management for external resources.

The addresses of the scheduling registers are listed in **table 1.** The unused six bits will read all "0".

Status Diagram of the Scheduling Registers



Notes :
1) The owner bit shows who accessed the register last.
2) During simultaneous access, port 1 has priority.
3) A write is only possible if the respective port is "owner" of the register.

Figure 1

Oscillator Watchdog

This output provides a means to control the oscillator circuit and the crystal.
Whenever the clock frequency drops below a threshold of approx. 100 kHz, this output switches to low.

Timer

The three timers are 24-bit counters with a clock frequency of $f_{CLK}/6$. Each of the counters can be set by writing to 3 specific RAM addresses. The value is simultaneously stored in the RAM and in a buffer register of the timer. When writing to the low byte, all three bytes are transferred to the reload register. The value in the reload register is maintained in all modes until the corresponding low byte is written again. The counters are down counters. The counters can be started by setting bit 7 in the corresponding TMR. Additionally, counter 3 can be started by an external trigger signal (TS 3). Each counter can be configured by a timer mode register (TMR). The meaning of the bits of the TMR is described below.

Bit 0: Protects the reload register against overwriting.
Application: After writing to the reload register, the parallel RAM region can be used after the timer is started – by writing to the corresponding protection bit – without influencing the reload register (reset state = 0).

Bit 4: Serves to switch output signal polarity (reset state = 0)
Bit 4 = 0; idle state 1, active 0
Bit 4 = 1; idle state 0, active 1

Bit 5: Selects the mode (reset state = 0):
Bit 5 = 0 single shot, i.e. when the counter is started, the output signal goes active. After zero is reached, the output signal returns to idle. To generate another count period, the timer must be started again. During this, the values from the reload register are loaded into the counter.
Bit 5 = 1 auto-reload, i.e. the value of the reload register is loaded into the counter when the counter is started. When reaching zero, the counter outputs a pulse (~4 µs) and reloads the old value automatically, starting the process again, so that a frequency can be adjusted with a 24-bit resolution. If a new start pulse occurs during the counting period (even without "STOP"), no pulse is output and the counter is reloaded.

Bit 6: In the reload mode the timer can be stopped by setting this bit. (During a new start the contents of the counter are lost, but not the contents of the reload register).

Bit 7: Setting this bit starts the counter.

Only for Timer 1 and 2

Bit 1-3: In conjunction with bit 0 serve to switch the watchdog mode on or off.

Only for Timer 3

Bit 1-2: Reserved (must always be 0 for proper operation)

Bit 3: Switches **all 3** timers to test mode, i.e. only the upper 12 bits are used to generate the output signal. (Reset state = 0).

Watchdog Mode

A special mode is provided for timers 1 and 2, which can be used to monitor the two processors that are connected. For this mode, an additional register **(address see table 1)** – referred to as control register (CR) in the following – is used per timer. Watchdog mode is enabled by loading the TMR with the value "$101X1111_B$", bit 4 being used to freely select the polarity of the output signal. This mode operates in a similar manner as the auto-reload mode, except that in this case, neither the contents of the reload register nor the TMR can be changed.

In the watchdog mode the timer can only be restarted (and thus suppressing the output pulse) when first 055_H and then $0AA_H$ is written into the control register. There is no time limit between these two write accesses, however no other value must be written into the timer mode register nor into the control register between these two operations, otherwise the sequence must be started again.

In order to reset the timer into the normal mode, the following sequence must be performed. First the value 055_H must be written into the control register, then the value $011X0000_B$ into the TMR, and finally the value $0AA_H$ into the control register. The same condition applies for this sequence; if any other value is written into one of the two registers, the total operation must be started over again. There is no time limit between the accesses.

The appendix shows the operation of the timer in watchdog mode as an example program for the 8051.

Figure 2: Bit Assignment of the Timer Mode Registers for Timer 1 and Timer 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (= 1)	Timer stop (= 1) for auto-reload	Mode (auto-reload = 1 single shot = 0)	Polarity of the output pulse (high = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Protection (=1) write protects the reload register

Figure 3: Bit Assignment of the Timer Mode Register for Timer 3

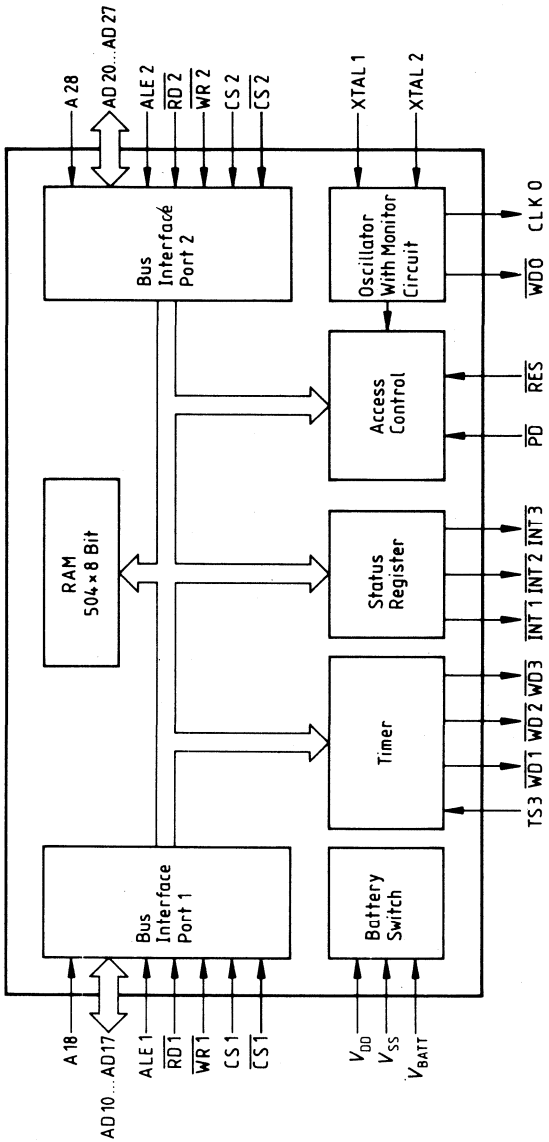
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (= 1)	Timer stop (= 1) for auto-reload	Mode (auto-reload = 1 single shot = 0)	Polarity of the output pulse (high = 0)	Test (= 1) switches timer into test mode	Reserved (normal mode = 0)	Reserved (normal mode = 0)	Protection (=1) write protects the reload register

Address Assignment of the DPR Registers (Preliminary)

Register		Address
Scheduling register	1	$1F8_H$
Scheduling register	2	$1F9_H$
Scheduling register	3	$1FA_H$
Scheduling register	4	$1FB_H$
Scheduling register	5	$1FC_H$
Scheduling register	6	$1FD_H$
Scheduling register	7	$1FE_H$
Scheduling register	8	$1FF_H$
Timer mode register	1	$1E0_H$
Timer mode register	2	$1E4_H$
Timer mode register	3	$1E8_H$
High byte timer	1	$1E3_H$
Medium byte timer	1	$1E2_H$
Low byte timer	1	$1E1_H$
High byte timer	2	$1E7_H$
Medium byte timer	2	$1E6_H$
Low byte timer	2	$1E5_H$
High byte timer	3	$1EB_H$
Medium byte timer	3	$1EA_H$
Low byte timer	3	$1E9_H$
Control register timer	1	$1EC_H$
Control register timer	2	$1ED_H$
Interrupt output	1	$1F8_H$
Interrupt output	2	$1F9_H$
Interrupt output	3	$1FA_H$

Table 1

Block Diagram



Maximum Ratings

$T_A = -40$ to $+85$ °C

		min.	typ.	max.	Unit
Supply voltage	V_{DD}	−0.3		6	V
Input voltage	V_R	−0.3		V_{DD} +0.3	V
Power dissipation per output	P_Q			50	mW
Total power dissipation	P_{tot}			500	mW
Storage temperature	T_{stg}	−50		125	°C

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (without output loading)	I_{DD}			20	mA
Operating frequency	f_s			12	MHz
Ambient temperature	T_A	−40		+85	°C
Standby current	I_{DD}, I_{BATT}			1	µA
Data retention voltage	V_{DR}	1			V
Battery voltage (referred to V_{DD}) (with sufficiently low internal impedance)	V_{BATT}	−1		−3	V

Maximum Ratings

Maximum ratings are absolute ratings. Exceeding even one of them may result in the destruction of the integrated circuit. All voltages refer to V_{SS}.

Operating Range

Within the operating range the functions mentioned in the circuit description will be fulfilled. Deviations from the characteristics are possible. All voltages refer to V_{SS}.

Characteristics

$T_A = 25\,°C$

		min.	max.	Unit
All input signals				
H input voltage	V_{IH}	2.2	V_{DD}	V
L input voltage	V_{IL}	0	0.8	V
Input capacitance	C_I		10	pF
Input current	I_I		1	µA
Output signals AD10-17, AD20-27				
H output voltage $I_Q = 0.5$ mA	V_{QH}	2.4	V_{DD}	V
L output voltage $I_Q = 1.6$ mA	V_{QL}	V_{SS}	0.4	V
Output signals $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$, $\overline{WDO}$ (Open-drain outputs)				
L output voltages $I_Q = 1.6$ mA	V_{QL}	V_{SS}	0.4	V
Output signal CLKO				
H output voltage $I_{QH} = 0.5$ mA	V_{QH}	2.4	V_{DD}	V
L output voltage $I_{QL} = 1.6$ mA	V_{QL}	V_{SS}	0.4	V
Load capacitance	C_L		80	pF

DC Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_A = 25\,°C$ and mean supply voltage. All voltages refer to V_{SS}.

AC Characteristics

$T_A = 25\,°C$

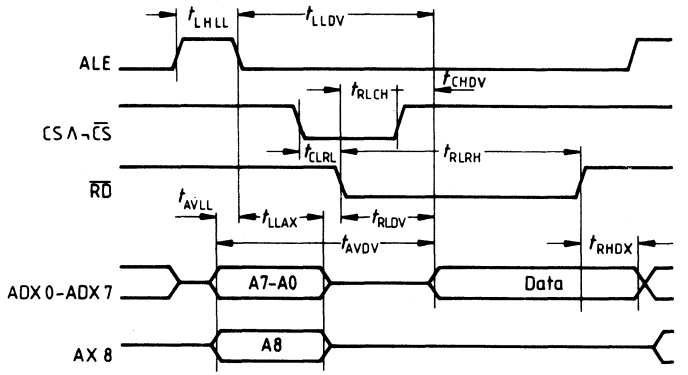
		min.	max.	Unit
ALE pulse width	t_{LHLL}	60		ns
Address setup to ALE low	t_{AVLL}	30		ns
Address hold time after ALE low	t_{LLAX}	40		ns
$\overline{RD}$ pulse width	t_{RLRH}	2 T_{OSC} +20		ns
$\overline{WR}$ pulse width	t_{WLWH}	2 T_{OSC} +20		ns
ALE low to $\overline{RD}$ or $\overline{WR}$ active	t_{LLWL}	60		ns
$\overline{RD}$ active valid data out (chip select active)	t_{RLDV}		2 T_{OSC}	ns
Data hold after $\overline{RD}$ inactive	t_{RHDX}		30	ns
ALE low to valid data out	t_{LLDV}		3 T_{OSC} +20	ns
Valid data in after $\overline{WR}$ low	t_{DVWL}	1/2 T_{OSC}	2 T_{OSC}*)	ns
$\overline{WR}$ low to ALE high	t_{WLLL}	3 T_{OSC}		ns
Data setup before $\overline{WR}$ high	t_{QVWH}	30		ns
Data hold after $\overline{WR}$ high	t_{WHQX}	40		ns
Delay $\overline{RD}$ low to both chip selects active	t_{RLCH}		40	ns
Delay $\overline{WR}$ low to both chip selects active	t_{WLCH}		40	ns
Chip-select setup to $\overline{RD}$	t_{CLRL}	0		ns
Chip-select setup to $\overline{WR}$	t_{CLWL}	0		ns
Active pulse width of timer outputs	t_{ACT}	48 T_{OSC}		ns
Pulse width TS 3	t_{THTL}	2 T_{OSC}		ns
Oscillator pulse width	t_{OSC}	83		ns
High time	t_{OSCH}	25		ns
Low time	t_{OSCL}	25		ns
Rise time	t_r		40	ns
Fall time	t_f		40	ns

The AC characteristics apply throughout the operating range.

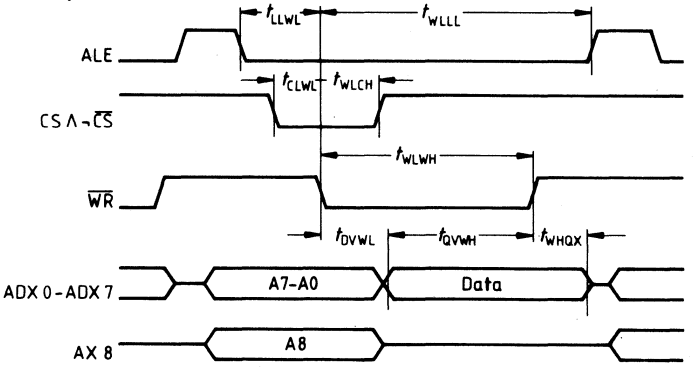
*) Only applies if the $\overline{WR}$ signal is longer than 2 T_{OSC}.
Changes of the data bus signals after this time will have no effect.

Pulse Diagrams

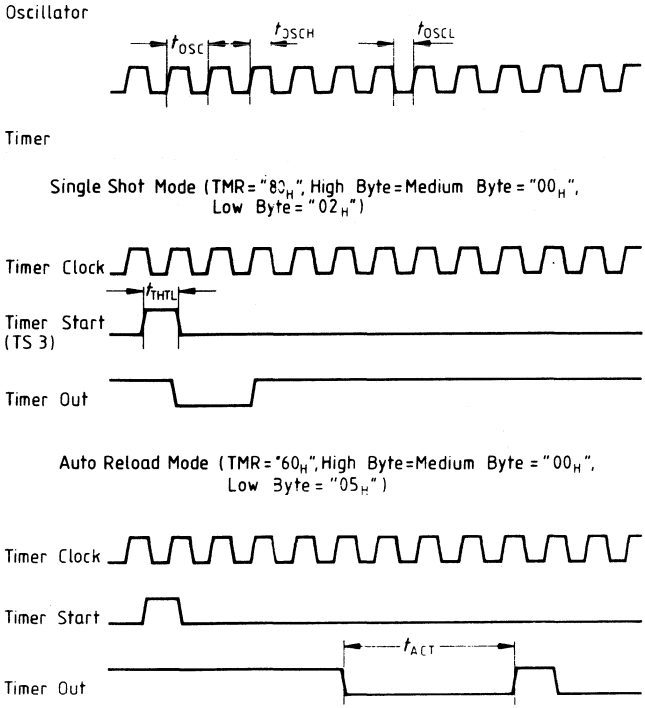
Read Cycle



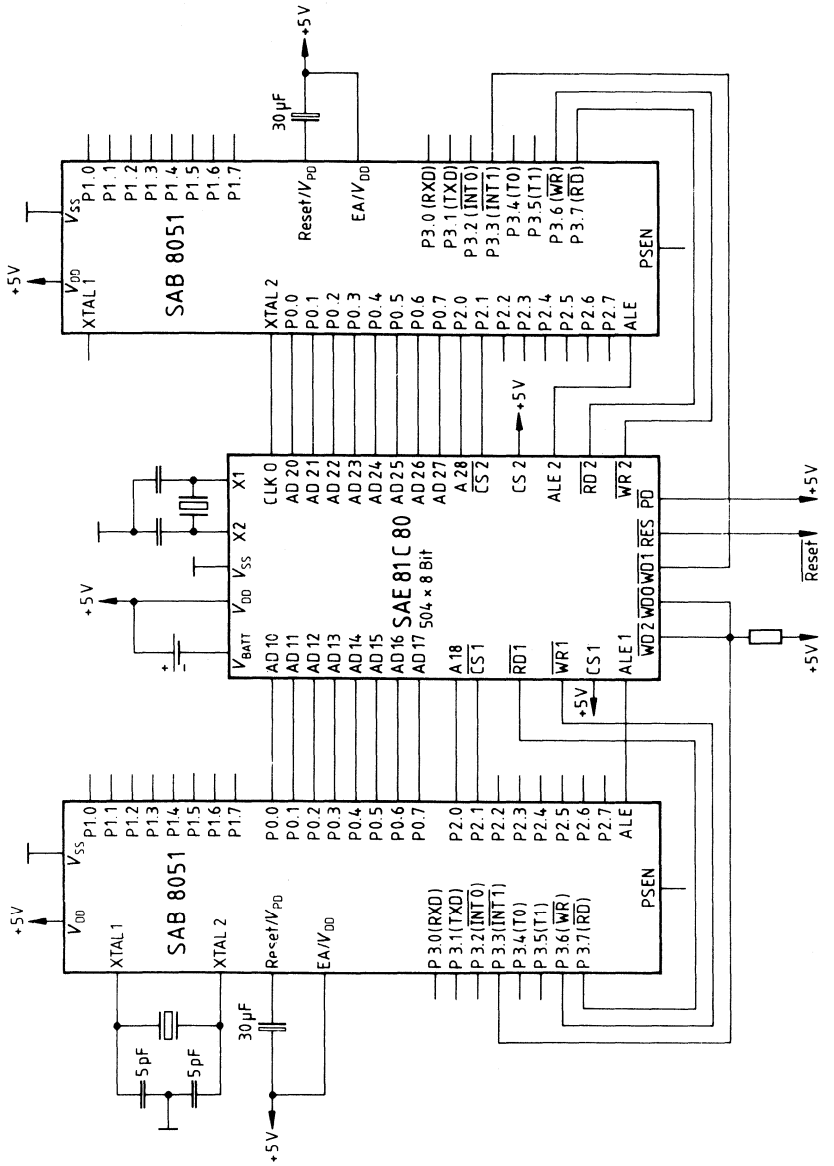
Write Cycle



Pulse Diagram



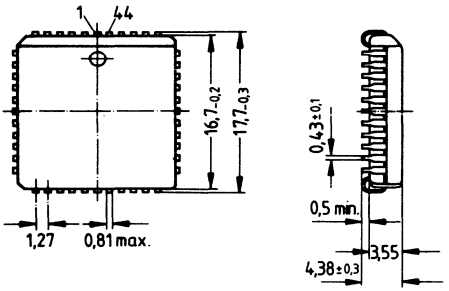
Application Circuit



8051 – Program for Timer Operation in Watchdog Mode

```
HBYTE   EQU   1E3H    : Address high byte reload register
TMR     EQU   1E0H    : Address timer mode register
KR      EQU   1ECH    : Address control register
REST1   EQU   055H    : 1 value to restart timer
REST2   EQU   0AAH    : 2 value to restart timer
WDAUS   EQU   060H    : Value to switch off watchdog mode

: Load reload register

MOV     DPTR, # HBYTE
CLR     A
MOVX    @ DPTR,A
DEC     DPL
MOV     A, # 0FFH
MOVX    @ DPTR,A
DEC     DPL
MOVX    @ DPTR,A

: Switch on watchdog mode and start timer

MOV     A, # 0AFH
DEC     DPL
MOVX    @ DPTR,A

: Reset timer

MOV     DPTR, # KR
MOV     A, # REST1
MOVX    @ DPTR,A
MOV     A, # REST2
MOVX    @ DPTR,A

: Switch off watchdog mode and stop timer

MOV     DPTR, # KR
MOV     A, # REST1
MOVX    @ DPTR,A
MOV     A, # WDAUS
MOV     DPTR, # TMR
MOVX    @ DPTR,A
MOV     A, # REST2
MOV     DPTR, # KR
MOVX    @ DPTR,A

;

END
```

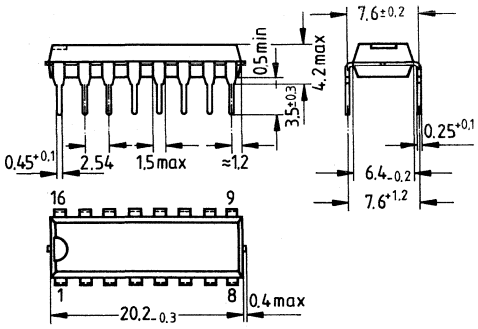
Plastic Package, PLCC,
44 pins (SMD)



Dimensions in mm

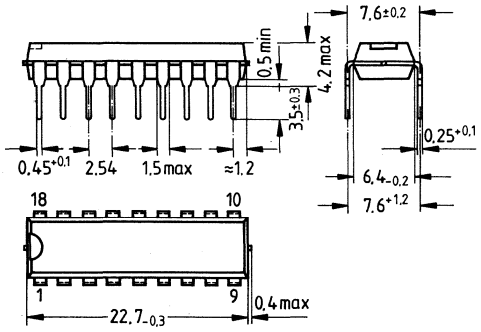
Summary of Package Outlines

Plastic Package, P-DIP-16
(dual-in-line package)



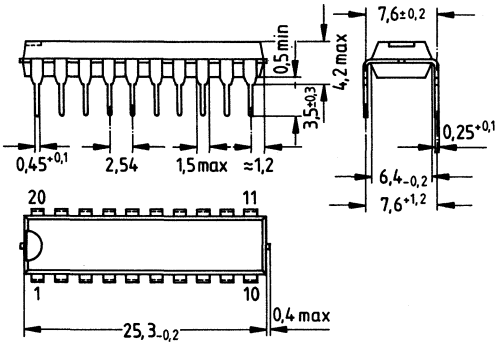
Dimensions in mm

Plastic Package, P-DIP-18
(dual-in-line package)



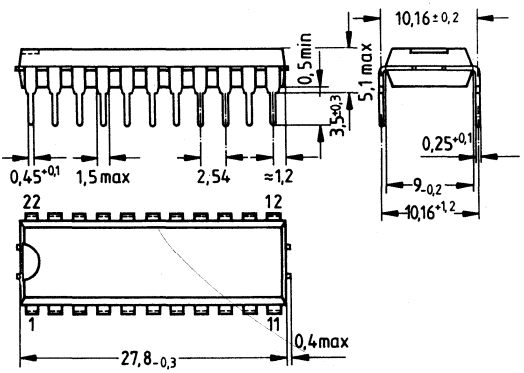
Dimensions in mm

Plastic Package, P-DIP-20
(dual-in-line package)



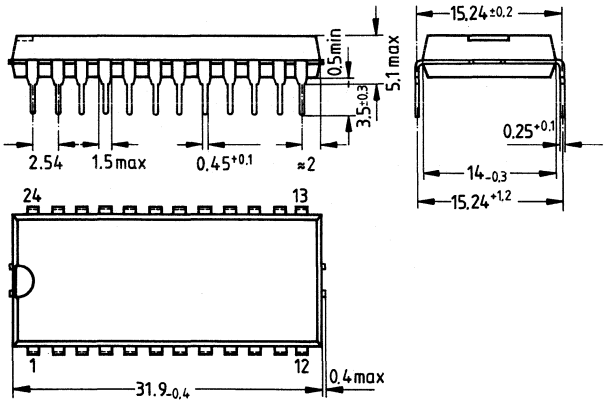
Dimensions in mm

Plastic Package, P-DIP-22
(dual-in-line package)



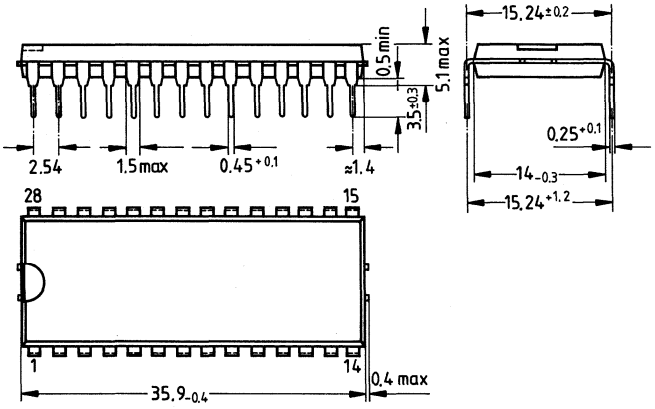
Dimensions in mm

Plastic Package, P-DIP-24
(dual-in-line package)



Dimensions in mm

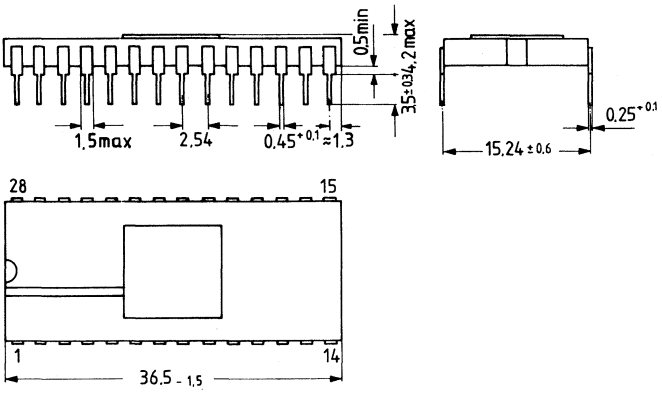
Plastic Package, P-DIP-28
(dual-in-line package)



Dimensions in mm

Package Outlines

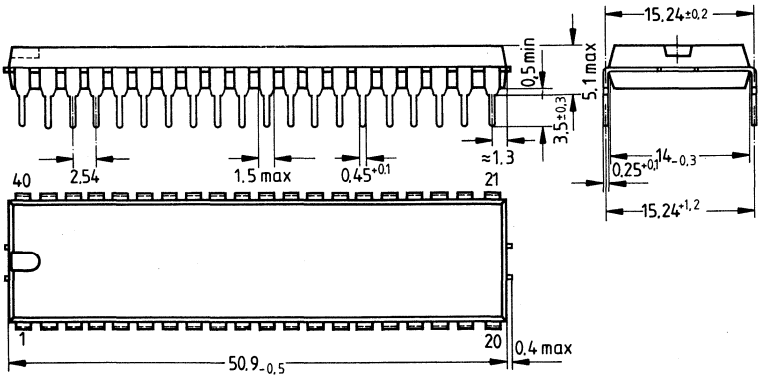
Ceramic Package, C-DIP-28
(dual-in-line package)



Gewicht etwa 3,5 g

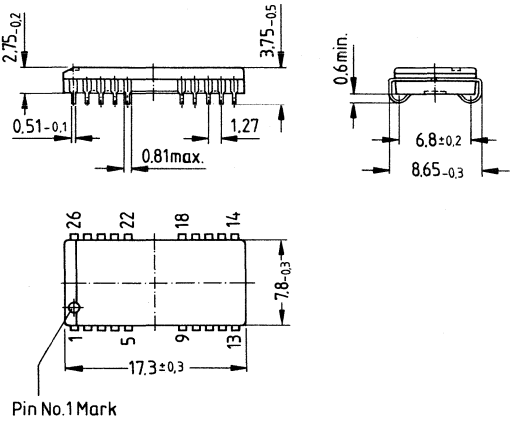
Dimensions in mm

Plastic Package, P-DIP-40
(dual-in-line package)



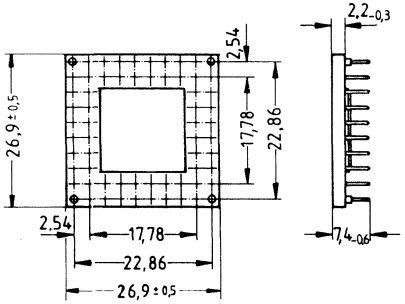
Dimensions in mm

Plastic Package, P-SOJ-26-20



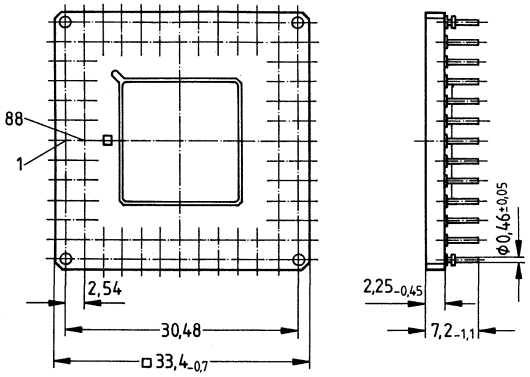
Dimensions in mm

Ceramic Package, C-PGA-64
(pin-grid-array)



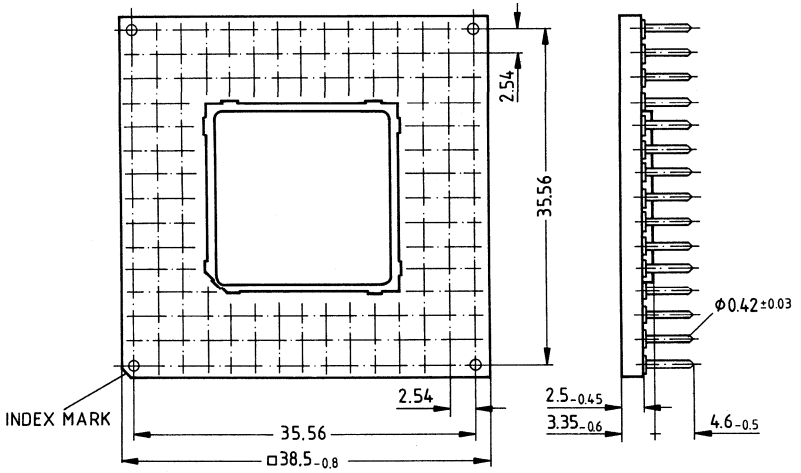
Dimensions in mm

Ceramic Package, C-PGA-88
(pin-grid-array)



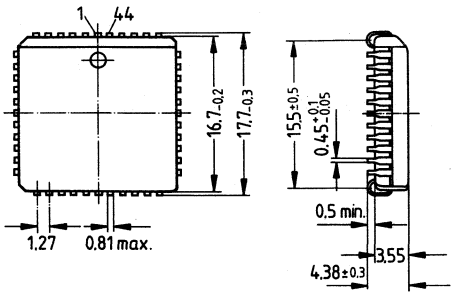
Dimensions in mm

Ceramic Package, C-PGA-145
(pin-grid-array)



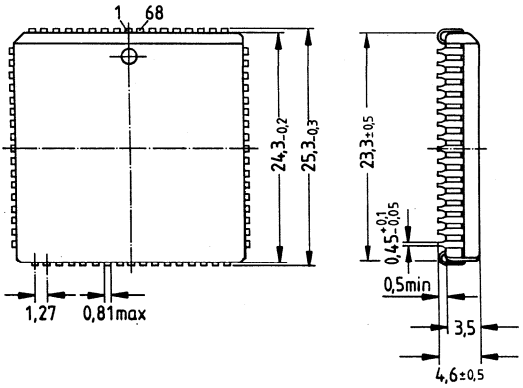
Dimensions in mm

Plastic Package, PL-CC-44
(chip-carrier) - SMD



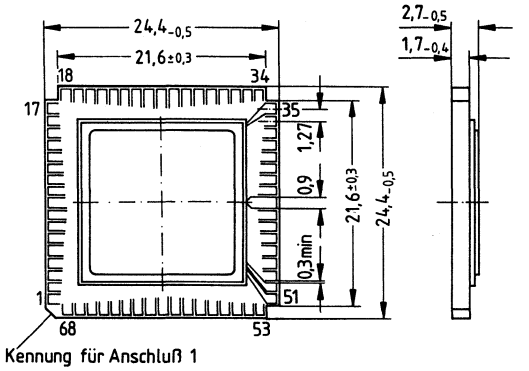
Dimensions in mm

Plastic Package, PL-CC-68
(chip-carrier) - SMD



Dimensions in mm

Plastic Package, C-CC-68
(chip-carrier) - SMD



Dimensions in mm

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